S1D19105 Series

Rev.1.1

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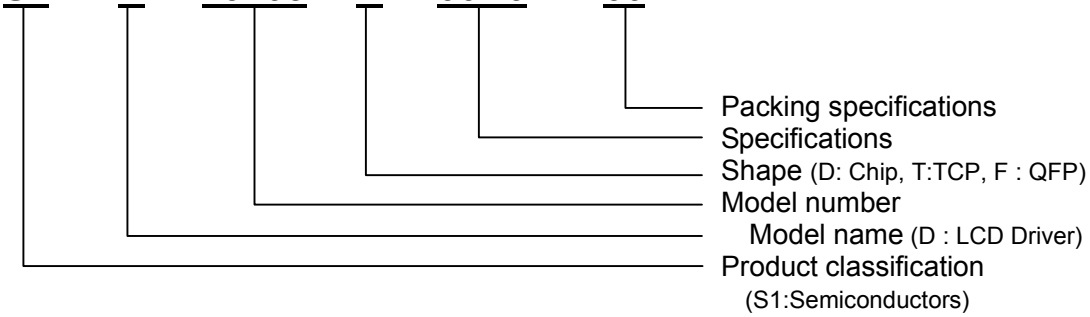
Configuration of product number

●DEVICES

S1 D 19105 D 00B0 00



CONTENTS

1. DESCRIPTION

The S1D19105 series is a 1-chip driver for driving amorphous Si-TFT with built-in data RAM that contains 176 RGB × 220 dots, supporting 262k-color display. Since this series contains all power circuits necessary for the 220-output gate driver, 176-RGB output source driver, and the display, the TFT color panel module of a maximum of 176 RGB × 220 dots can be constructed with a minimum of components.

The S1D19105 incorporates 8/9/16/18-bit parallel interface that can be directly attached to the micro computer (hereafter referred to as MPU) bus. The 3-line serial interface can also be used. The S1D19105 series receives parallel or serial display data from the microprocessor, stores it in the display data RAM, and outputs resource line drive signals, gate driver drive signals, and AC operation timing signals independent from MPU operations. Also, for movie display, 6/16/18-bit RGB interface and VSYNC synchronization function are provided.

The S1D19105 series has the low current consumption, source line drive circuit (including reference voltage adjustment resistor and bias circuit for reference voltage circuit), high-efficiency power circuit and the CR oscillation circuit for fully-built-in display clock that does not require external parts. In addition, power can be controlled more finely using command control, as this series supports 8-color display mode and partial display mode. The S1D19105 series provides a high-performance but handy display system with a minimum of components in the minimum power consumption.

2. FEATURES

- Supports 176 RGB × 220 dots and 262,144 colors amorphous Si-TFT color panel.
- RAM capacity 176 × 3 × 220 × 6 = 696,960 bits
- Display function

Display of 262k-color at a time
Area scrolling
Partial display
8-color display mode

- Interface function

Selection from 8/9/16/18-bit parallel MPU interface.
Direct attachment to either of 80- and 68-series MPUs.
262k-color display via 16-bit interface by selecting 2+16 and 16+2 modes.
Serial interface 3 signal lines ($\overline{CS}$, SCL, and SI signals)
Selection from 6/16/18-bit RGB interface specifically for moving picture display, etc.
VSYNC synchronization function provides flicker-free moving picture display.

- 176 × 3 source line drive output A 6-bit D/A converter is included.
- A 110 output each is placed on the right and left sides of the 220 gate line drive output chip. Also, supports interlace drive.
- CR oscillation circuit (External clocks can also be used.)
- Common electrode drive signal outputs (V_{COM} signals)

Allows 1-frame/3-line interlace/n-line reverse driving.

- Low supply voltage operation

V_{DDI} - V_{SS} = 1.65 to 3.3V (interface I/O power supply)
V_{DD} - V_{SS} = 2.3 to 3.1V (power supply for internal logic power supply)
V_{DD2} - V_{SS} = 2.3 to 3.1V (power supply for built-in power circuits)
V_{DDCORE} - V_{SS} = 2.3 to 3.1V (internal logic power supply)
Source voltage = Max.5.5V
Gate voltage = Max.30V

- BUMP layout appropriate for COG assembly
- Package models available: Au bump chip and COF

3. BLOCK DIAGRAM

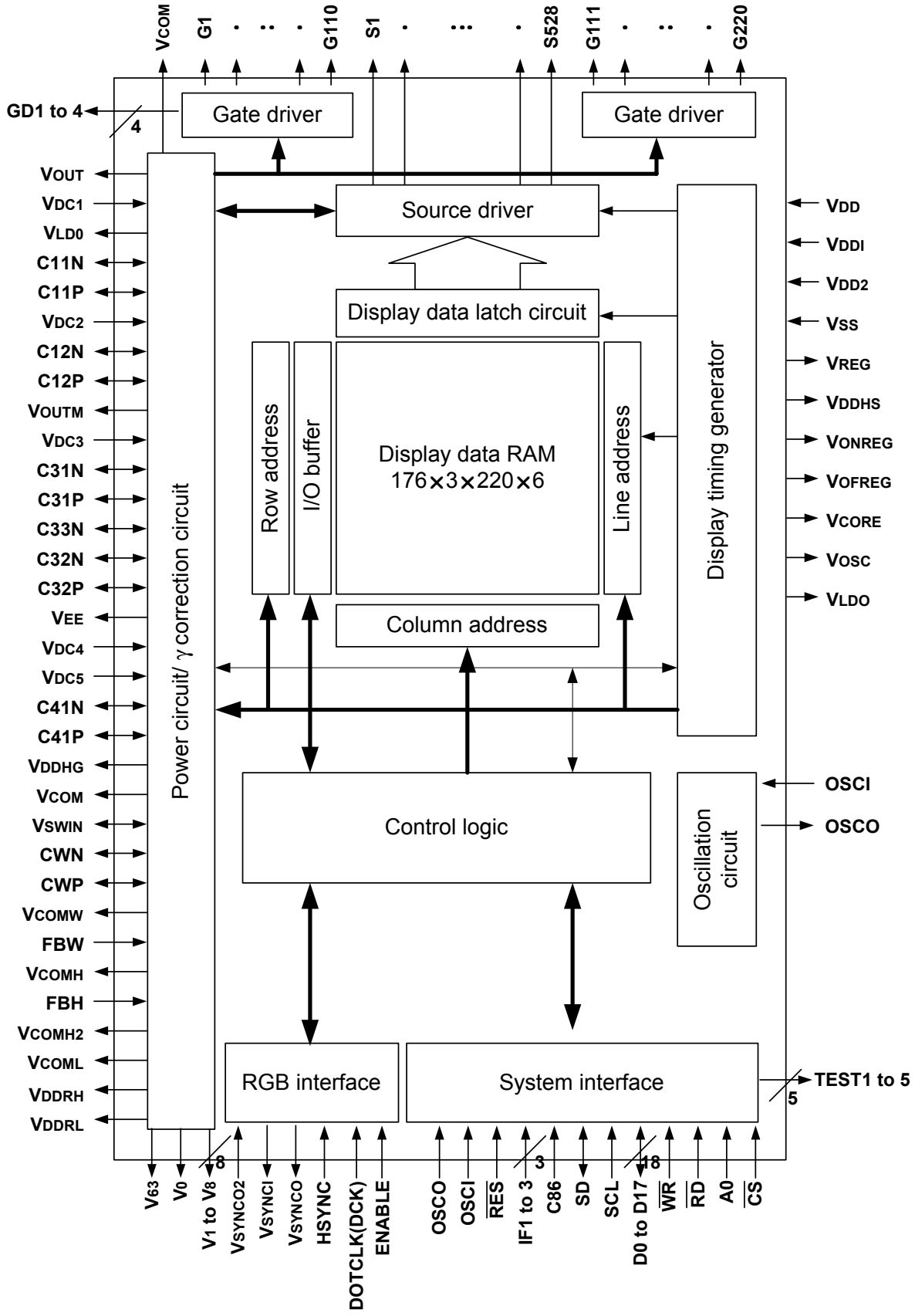


Fig.1 S1D19105 Series Block Diagram

4. PIN ASSIGNMENT

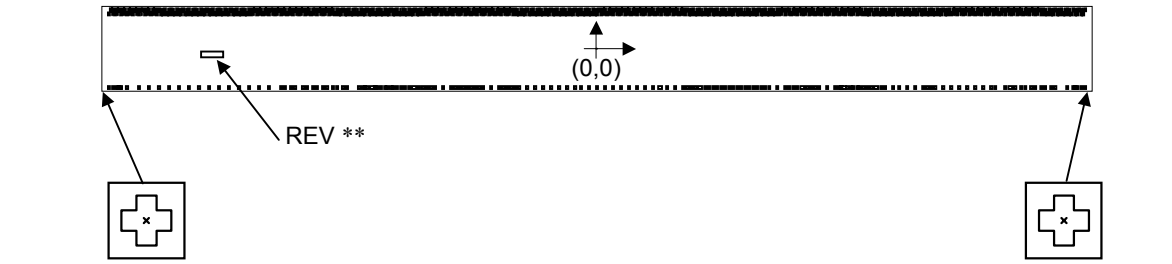
4.1 S1D19105 Specifications of Chip

Table 1 Specifications of Chip

Parameter		Dimensions		Unit
		X	Y	
Chip size		19.56	2.49	mm
Chip thickness		400		µm
Bump pitch		Min.50		µm
Bump size	No.1 to 205	54	100	µm
	No.206 to 978	24	105	µm
Bump height		Typ.15		µm

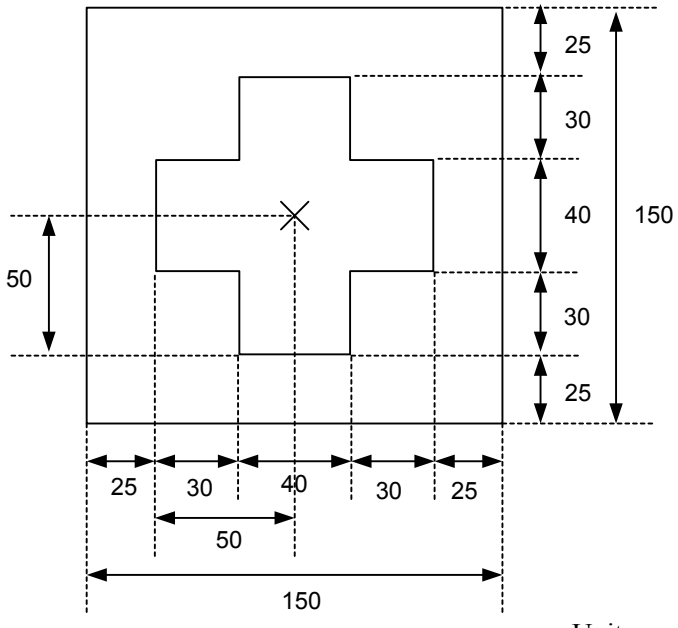
Note: These values are given for reference only.

Table 2 Bump Assignment Drawing



(Coordinate 1: -9593.0, -1079.1) (Coordinate 2: 9593.0, -1079.1)

The alignment mark is put on two locations.

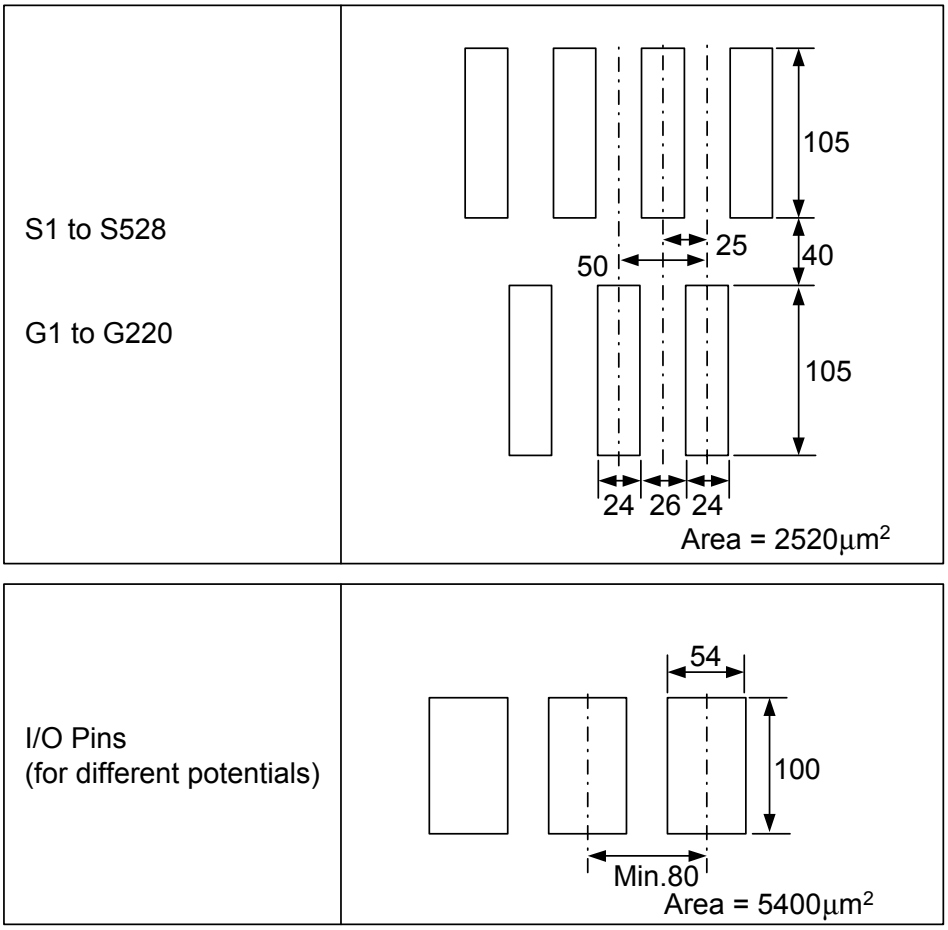


Unit: µm

Fig.2 Alignment Mark

Unit: μm

Fig.3 Revision Coordinate Mark



Unit: μm

Fig.4 Bump Size and Assignment Drawing

4.2 Bump Center Coordinates

Table 3 Bump Center Coordinates

Unit: μm

BUMP No.	Signal name	X	Y
1	ADUMMY	-9429.2	-1098.6
2	BDUMMY	-9349.2	↓
3	DUMMY	-9269.2	↓
4	V_{COM}	-9189.2	↓
5	V_{COM}	-9109.2	↓
6	DUMMY	-9029.2	↓
7	V_{DDHG}	-8949.2	↓
8	V_{DDHG}	-8869.2	↓
9	DUMMY	-8789.2	↓
10	C41P	-8709.2	↓
11	C41P	-8629.2	↓
12	DUMMY	-8549.2	↓
13	C41N	-8469.2	↓
14	C41N	-8389.2	↓
15	DUMMY	-8309.2	↓
16	V_{ONREG}	-8229.2	↓
17	V_{DC4}	-8149.2	↓
18	V_{DC5}	-8039.2	↓
19	V_{OFREG}	-7929.2	↓
20	V_{DC3}	-7819.2	↓
21	V_{OUTDM}	-7739.2	↓
22	C32P	-7649.2	↓
23	C32P	-7569.2	↓
24	C32N	-7435.5	↓
25	C32N	-7355.5	↓
26	DUMMY	-7275.5	↓
27	V_{EE}	-7195.5	↓
28	V_{EE}	-7115.5	↓
29	C33N	-7025.5	↓
30	C33N	-6945.5	↓
31	DUMMY	-6865.5	↓
32	C31N	-6785.5	↓
33	C31N	-6705.5	↓
34	C31P	-6571.8	↓
35	C31P	-6491.8	↓

BUMP No.	Signal name	X	Y
36	V_{CORE}	-6411.8	-1098.6
37	V_{CORE}	-6331.8	↓
38	V_{CORE}	-6251.8	↓
39	V_{CORE}	-6171.8	↓
40	V_{DDI}	-6091.8	↓
41	V_{DDI}	-6011.8	↓
42	V_{SS}	-5931.8	↓
43	V_{SS}	-5851.8	↓
44	V_{SS}	-5771.8	↓
45	V_{SS}	-5691.8	↓
46	C86	-5611.8	↓
47	IF1	-5531.8	↓
48	IF2	-5451.8	↓
49	IF3	-5371.8	↓
50	DUMMY	-5291.8	↓
51	V_{63}	-5211.8	↓
52	V_8	-5131.8	↓
53	V_7	-5051.8	↓
54	V_6	-4971.8	↓
55	V_5	-4891.8	↓
56	V_4	-4811.8	↓
57	V_3	-4731.8	↓
58	V_2	-4651.8	↓
59	V_1	-4571.8	↓
60	V_0	-4491.8	↓
61	DUMMY	-4411.8	↓
62	$\overline{RES}$	-4331.8	↓
63	DUMMY	-4251.8	↓
64	$\overline{CS}$	-4171.8	↓
65	DUMMY	-4091.8	↓
66	A0	-4011.8	↓
67	DUMMY	-3931.8	↓
68	$\overline{WR}$	-3851.8	↓
69	DUMMY	-3771.8	↓
70	$\overline{RD}$	-3691.8	↓

Unit: µm

BUMP No.	Signal name	X	Y
71	DUMMY	-3611.8	-1098.6
72	D0	-3531.8	
73	D1	-3371.8	
74	D2	-3211.8	
75	D3	-3051.8	
76	D4	-2891.8	
77	D5	-2731.8	
78	D6	-2571.8	
79	D7	-2411.8	
80	D8	-2251.8	
81	D9	-2091.8	
82	D10	-1931.8	
83	D11	-1771.8	
84	D12	-1611.8	
85	D13	-1451.8	
86	D14	-1291.8	
87	D15	-1131.8	
88	D16	-971.8	
89	D17	-811.8	
90	DUMMY	-651.8	
91	VSYNCO2	-491.8	
92	VSYNCO	-331.8	
93	VSYNCI	-171.8	
94	DUMMY	-91.8	
95	HSYNC	-11.8	
96	DUMMY	68.2	
97	DCK	148.2	
98	DUMMY	228.2	
99	ENABLE	308.2	
100	DUMMY	388.2	
101	DUMMY	468.2	
102	DUMMY	548.2	
103	DUMMY	628.2	
104	SCL	708.2	
105	DUMMY	788.2	↓

BUMP No.	Signal name	X	Y
106	SD	868.2	-1098.6
107	EECK	1028.2	
108	EEDA	1188.2	
109	EECS	1348.2	
110	V_{EP}	1508.2	
111	TEST1	1668.2	
112	DUMMY	1748.2	
113	TEST2	1828.2	
114	DUMMY	1908.2	
115	TEST3	1988.2	
116	DUMMY	2068.2	
117	TEST4	2148.2	
118	DUMMY	2228.2	
119	TEST5	2308.2	
120	DUMMY	2388.2	
121	TRI	2468.2	
122	OSCO	2548.2	
123	OSCI	2628.2	
124	V_{OSC}	2708.2	
125	V_{DDRL}	2798.2	
126	V_{DDRH}	2908.2	
127	V_{REG}	2998.2	
128	V_{SS}	3088.2	
129	V_{SS}	3168.2	
130	V_{SS}	3248.2	
131	V_{SS}	3328.2	
132	V_{SS}	3408.2	
133	V_{SS}	3488.2	
134	V_{SS}	3568.2	
135	V_{SS}	3648.2	
136	V_{DDI}	3728.2	
137	V_{DDI}	3808.2	
138	V_{DDI}	3888.2	
139	V_{DDI}	3968.2	
140	V_{CORE}	4048.2	↓

4. PIN ASSIGNMENT

Unit: µm

BUMP No.	Signal name	X	Y
141	VCORE	4128.2	-1098.6
142	VCORE	4208.2	
143	VCORE	4288.2	
144	VCORE	4368.2	
145	VCORE	4448.2	
146	VCORE	4528.2	
147	VCORE	4608.2	
148	VDD	4688.2	
149	VDD	4768.2	
150	VDD	4848.2	
151	VDD	4928.2	
152	VDD	5008.2	
153	VDD	5088.2	
154	VDD	5168.2	
155	VDD	5248.2	
156	VDD2	5328.2	
157	VDD2	5408.2	
158	VDD2	5488.2	
159	VDD2	5568.2	
160	VDD2	5648.2	
161	VDD2	5728.2	
162	VDD2	5808.2	
163	VDD2	5888.2	
164	VDC1	5968.2	
165	VDC1	6048.2	
166	VLDO	6128.2	
167	VLDO	6208.2	
168	C11N	6288.2	
169	C11N	6368.2	
170	C11N	6448.2	
171	C11N	6528.2	
172	C11P	6608.2	
173	C11P	6688.2	
174	C11P	6768.2	
175	C11P	6848.2	

BUMP No.	Signal name	X	Y
176	VOUT	6928.2	-1098.6
177	VOUT	7008.2	
178	VOUT	7088.2	
179	VOUT	7168.2	
180	VDDHS	7248.2	
181	VDDHS	7328.2	
182	VDC2	7408.2	
183	VDC2	7488.2	
184	C21P	7578.2	
185	C21P	7658.2	
186	C21N	7791.9	
187	C21N	7871.9	
188	VOUTM	7961.9	
189	VOUTM	8041.9	
190	VCOML	8121.9	
191	VCOML	8201.9	
192	VCOMH2	8335.6	
193	FBH	8415.6	
194	VREG	8495.6	
195	VCOMH	8575.6	
196	FBW	8655.6	
197	VCOMW	8735.6	
198	CWP	8815.6	
199	CWN	8895.6	
200	VSWIN	8975.6	
201	VCOM	9109.3	
202	VCOM	9189.3	
203	DUMMY	9269.3	
204	CDUMMY	9349.3	
205	DDUMMY	9429.3	

Unit: µm

BUMP No.	Signal name	X	Y
206	DUMMY	9650	958.8
207	DUMMY	9625	1103.8
208	VCOM	9600	958.8
209	VCOM	9575	1103.8
210	DDUMMY	9550	958.8
211	CDUMMY	9525	1103.8
212	GD1	9500	958.8
213	G1	9475	1103.8
214	G2	9450	958.8
215	G3	9425	1103.8
216	G4	9400	958.8
217	G5	9375	1103.8
218	G6	9350	958.8
219	G7	9325	1103.8
220	G8	9300	958.8
221	G9	9275	1103.8
222	G10	9250	958.8
	•	•	•
	•	•	•
	•	•	•
321	G109	6775	1103.8
322	G110	6750	958.8
323	GD2	6725	1103.8
324	DUMMY	6700	958.8
325	DUMMY	6675	1103.8
326	DUMMY	6650	958.8
327	DUMMY	6625	1103.8
328	S1	6600	958.8
329	S2	6575	1103.8
330	S3	6550	958.8
331	S4	6525	1103.8
332	S5	6500	958.8

BUMP No.	Signal name	X	Y
333	S6	6475	1103.8
334	S7	6450	958.8
335	S8	6425	1103.8
336	S9	6400	958.8
337	S10	6375	1103.8
	•	•	•
	•	•	•
	•	•	•
853	S526	-6525	1103.8
854	S527	-6550	958.8
855	S528	-6575	1103.8
856	DUMMY	-6600	958.8
857	DUMMY	-6625	1103.8
858	DUMMY	-6650	958.8
859	DUMMY	-6675	1103.8
860	DUMMY	-6700	958.8
861	GD3	-6725	1103.8
862	G111	-6750	958.8
863	G112	-6775	1103.8
864	G113	-6800	958.8
	•	•	•
	•	•	•
	•	•	•
970	G219	-9450	958.8
971	G220	-9475	1103.8
972	GD4	-9500	958.8
973	BDUMMY	-9525	1103.8
974	ADUMMY	-9550	958.8
975	VCOM	-9575	1103.8
976	VCOM	-9600	958.8
977	DUMMY	-9625	1103.8
978	DUMMY	-9650	958.8

X coordinates of Gm pin (m = 1 to 110): (110-m) × 25 + 6750µm
Y coordinates: m = 1103.8µm for odd number m = 958.8 µm for even number
X coordinates of Sm pin (m=1 to 528): (528-m) × 25 -6575µm
Y coordinates: m = 1103.8µm for odd number m = 958.8µm for even number
X coordinates of Gm pin (m=111 to 220): (220-m) × 25 -9475µm
Y coordinates: m = 1103.8µm for odd number m = 958.8µm for even number

5. PIN DESCRIPTION

5.1 External Power Pins

Table 4 External Power Pins

Pin Name	I/O	Connected To	Description	Number of pins
V_{DD2}	Power supply I	External power	Power pins for built-in power circuits. Used for built-in power supply. Used as the reference power supply for the 1st booster. Supply external power. See section 6.7 How to Connect to External Power Supply.	8
V_{DD}	Power supply I	External power	Power pins for V_{CORE} generation built-in power circuits. It is common to the V_{DD2}. Supply external power. See section 6.7 How to Connect to External Power Supply.	8
V_{DDI}	Power supply I	External power	Power pins dedicated to interface. Power supply for interface pins. Supply external power. See section 6.7 How to Connect to External Power Supply.	6
V_{SS}	Power supply I	External power	They are ground pins. The 0V pin connected to the system ground. Used as the IC board potential.	12

5.2 Built-in Power Pins

Table 5 Built-in Power Pins

Pin Name	I/O	Connected To	Description	Number of Pins
V_{CORE}	I/O	Capacity External power	Logic and RAM power supplies. Generated by a built-in power supply or connected to an external power. Connect it to external power basically. See section 6.7 How to Connect to External Power Supply.	12
V_{REG}	O	Capacity	Reference voltage for built-in power supply.	2
V_{DDHS}	O	Capacity	Voltage for generating source driver drive voltage.	2
V_{ONREG}	O	Capacity V_{DC4} Open	Voltage for adjusting V_{DDHG}. Connect it to capacity if it used. Set it to open if it is not used.	1
V_{OFREG}	O	Capacity V_{DC3} Open	Voltage for adjusting V_{EE}. Connect it to capacity if it used. Set it to open if it is not used.	1
V_{OSC}	O	Open	Voltage for CR oscillation circuit	1
V_{LDO}	O	Capacity Open	Used as the reference voltage for the 1st booster. Used to control the 1st booster voltage. Fixed it to open basically.	2
V_{DDRH}	O	Capacity	Reference voltage for V_0 generation for γ correction resistor.	1
V_{DDRL}	O	Capacity	Reference voltage for V_{63} generation for γ correction resistor.	1

5.3 1st Booster Pins

Table 6 1st Booster Pins

Pin Name	I/O	Connected To	Description	Number of Pins
V_{OUT}	O	Capacity	The 1st booster voltage. Outputs double V_{DC1} voltage for built-in power circuits.	4
V_{DC1}	I	V_{DD2} V_{LDO}	The 1st booster reference voltage input pin. Connect either V_{DD2} or V_{LDO}. Connect it to V_{DD2} basically.	2
C11N	I/O	Capacity	Flying capacitor for generating V_{OUT} output Connecting pins on the negative side	4
C11P	I/O	Capacity	Flying capacitor for generating V_{OUT} output Connecting pins on the positive side	4

5.4 The 2nd Booster Pins

Table 7 The 2nd Booster Pins

Pin Name	I/O	Connected To	Description	Number of Pins
V_{DC2}	I	V_{DD2} V_{OUT}	The 2nd booster reference voltage input pin. Connect either V_{DD2} or V_{OUT}.	2
C21P	I/O	Capacity	Flying capacitor for generating V_{OUTM} output Connecting pins on the positive side	2
C21N	I/O	Capacity	Flying capacitor for generating V_{OUTM} output Connecting pins on the negative side	2
V_{OUTM}	O	Capacity	Voltage for generating V_{COML} Outputs the voltage obtained by multiplying V_{DD2} or V_{OUT} by a factor of (-1).	2

5.5 The 3rd Booster Pins

Table 8 The 3rd Booster Pins

Pin Name	I/O	Connected To	Description	Number of Pins
V_{DC3}	I	V_{DD2} V_{OUTDM} V_{OFREG}	The 3rd booster reference voltage input pin. Connect it to either V_{OUTDM} or V_{OFREG}. Connect it to V_{OFREG} at the time of –3 times boosting.	1
V_{OUTDM}	O	V_{DC3} Open	Outputs V_{OUT}. Used to input V_{OUT} to V_{DC3}.	1
C31P	O	Capacity	1 Flying capacitor for generating V_{EE} output Connecting pins on the positive side	2
C31N	I/O	Capacity	1 Flying capacitor for generating V_{EE} output Connecting pins on the negative side	2
C33N	I/O	Capacity	3 Flying capacitor for generating V_{EE} output Connecting pins on the negative side	2
C32P	I/O	Capacity	2 Flying capacitor for generating V_{EE} output Connecting pins on the positive side	2
C32N	I/O	Capacity	2 Flying capacitor for generating V_{EE} output Connecting pins on the negative side	2
V_{EE}	O	Capacity	V_{EE} output pin Gate off voltage Outputs the voltage obtained by multiplying V_{DD2} or V_{OUT} by a factor of (-1 to -3).	2

5.6 The 4th Booster Pins

Table 9 The 4th Booster Pins

Pin Name	I/O	Connected To	Description	Number of Pins
V_{DC4}	I	V_{DD2} V_{SS} V_{ONREG}	The 4th booster reference voltage input pin. Connect it to V_{DD2}, V_{SS} or V_{ONREG}. It should be connected to V_{SS}. Because It is for discharge pin of the V_{DDHG}.	1
V_{DC5}	I	V_{DD2} V_{SS} V_{ONREG}	The 4th booster reference voltage input pin. Connect it to V_{DD2}, V_{SS} or V_{ONREG}.	1
C41P	I/O	Capacity	Flying capacitor connecting pins on the positive side for generating V_{EE} output	2
C41N	I/O	Capacity	Flying capacitor connecting pins on the negative side for generating V_{EE} output	2
V_{DDHG}	O	Capacity	V_{DDHG} output pin. Gate on voltage Outputs double boosted voltage between V_{DC4} and V_{EE} to V_{DC5}.	2

5.7 V_{COM} Generation Pins

Table 10 V_{COM} Generation Pins

Pin Name	I/O	Connected To	Description	Number of Pins
V_{SWIN}	O	Open	This pin. Fix it to open.	1
CWN	I/O	Open	This pin. Fix it to open.	1
CWP	I/O	Open	This pin. Fix it to open.	1
V_{COMW}	O	Open	This pin. Fix it to open.	1
FBW	I	Open	This pin. Fix it to open.	1
V_{COMH}	O	Capacity Resistor	Voltage output pin on the side of high voltage level of the VCOM signal. The twice of voltage inputted into the FBH pin are outputted. It is possible to adjust VCOMH voltage, maintaining VCOM amplitude by connecting variable resistance between VREG to VSS and inputting arbitrary voltage into FBH pin. Adjustment by the built-in electronic control is also possible.	2
FBH	I	VCOMH2 Resistor Capacity	It is an adjustment voltage input pin in the case of adjusting VCOMH voltage. When adjusting by external resistance, it is possible to adjust VCOMH voltage, maintaining VCOM amplitude by connecting variable resistance between VREG to VSS and inputting arbitrary voltage into FBH pin. The twice as many voltage inputted into the FBH pin as this is outputted to VCOMH. To adjust it using the built-in electronic control, connect it to the V_{COMH2} pin. Connect capacity about it between VSS to decrease the influence of the noise.	1
V_{COMH2}	O	FBH Open	This pin is used for connecting to FBH to adjust the V_{COMH} voltage with the built-in electronic control.	1
V_{COML}	O	Capacity	Voltage output pin on the side of low voltage level of the V_{COM} signal. $V_{COML}=V_{COMH} - VCA \times 2$ Outputs voltage by the above equation. VCA is the value of the built-in electronic control used for determining the amplitude of V_{COM}.	2

5.8 Control Pins

Table 11 Control Pins

Pin Name	I/O	Connected To	Description	Number of Pins
$\overline{CS}$	I	MPU	Chip Select pin. When $\overline{CS}$ = LOW, the pin is active and data or command input is enabled. In the test mode, clock input from the $\overline{CS}$ pin is enabled.	1
A0	I	MPU	Data/command identification pin When using the parallel interface, usually the least significant bit of the MPU address bus is connected to identify the data or command. When using the 9-bit serial interface, fix it for LOW or HIGH. A0= HIGH : The display data or command parameters are entered in the Data Bus pins. A0= LOW : The commands are entered in the Data Bus pins.	1
$\overline{RD}$ (E)	I	MPU	Read pin. (If connected to the 80-series MPU) While this signal is kept LOW, the data bus is output enabled at the $\overline{RD}$ signal pin of 80-series MPU. Enable clock pin. (If connected to the 68-series MPU) This is the Enable Clock input pin of the 68-series MPU. When the serial interface is selected, fix V_{DDI} or V_{SS} for the level.	1
$\overline{WR}$ (R/$\overline{W}$)	I	MPU	Write pin. (If connected to the 80-series MPU) Used for connecting 80-series MPU's $\overline{WR}$ signal. A signal on the data bus is latched at the rising edge of the $\overline{WR}$ signal. Read or write pin. (If connected to the 68-series MPU) This is the Read/Write signal input pin of the 68-series MPU. R/$\overline{W}$ = HIGH: Read R/$\overline{W}$ = LOW: Write When the serial interface is selected, fix V_{DDI} or V_{SS} for the level.	1
D0 to D17	I/O	MPU Controller	Data bus pin. 18-bit bi-directional data bus. Used as data bus for both parallel MUP interface and RGB interface. When the parallel MPU interface is selected and the Chip Select is in the non-active state, operations of all pins stop, disabling both input and output. The following signal pins are used for each mode. Unused pins can be set open. 8-bit mode D17 to D10 9-bit mode D17 to D9 16-bit mode D17 to D2 18-bit mode D17 to D0 Input pins used when the RGB interface is selected. The following signal pins are used for each mode. Unused pins can be set open. 6-bit mode D17 to D12 16-bit mode D17 to D2 18-bit mode D17 to D0	18

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Connected To</th><th>Description</th><th>Number of Pins</th></tr>
<tr><td>SCL</td><td>I</td><td>MPU</td><td>Serial clock pin.
Serial clock input pins used when the serial interface is selected.
When not choosing a serial interface, it is possible to make it to open.</td><td>1</td></tr>
<tr><td>SD</td><td>I/O</td><td>MPU</td><td>Serial data input/output pin.
Serial data input/output pin used when the serial interface is selected.
When not choosing a serial interface, it is possible to make it to open.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>VSS/
VDDI</td><td>MPU interface switching pin.
C86= HIGH : The 68-series MPU interface
C86= LOW : The 80-series MPU interface</td><td>1</td></tr>
<tr><td>IF1, IF2
IF3</td><td>I</td><td>VSS/
VDDI</td><td>MPU interface switching pin.
<table>
<tr><th>IF3</th><th>IF2</th><th>IF1</th><th>Interface</th></tr>
<tr><td>LOW</td><td>LOW</td><td>LOW</td><td>16-bit parallel</td></tr>
<tr><td>LOW</td><td>LOW</td><td>HIGH</td><td>18-bit parallel</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>LOW</td><td>8-bit parallel</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>HIGH</td><td>9-bit parallel</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>HIGH</td><td>9-bit serial</td></tr>
</table></td><td>3</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>MPU</td><td>Reset pin.
Resets if set to LOW.</td><td>1</td></tr>
<tr><td>OSCI</td><td>I</td><td>VSS/
VDDI</td><td>Clock input pin.
Test pin. Connect it to either VSS or VDDI.
When the built-in oscillation circuit is used, set (P17 data set command is “0”) and connect it to VSS or VDDI. When the built-in oscillation circuit is used, set (P17 data set command is “1”) and enter an external clock.</td><td>1</td></tr>
<tr><td>OSCO</td><td>O</td><td>Open</td><td>Clock output pin.
Test pin. Set open.
Outputs oscillation clocks when the built-in oscillator circuit is used.
Verifies the oscillation out when testing.</td><td>1</td></tr>
</table>

5.9 γ Reference Output Pin

Table 12 γ Reference Output Pin

Pin Name	I/O	Connected To	Description	Number of Pins
V_0	O	Capacity	MSB of the gray scale voltage	1
V_{63}	O	Capacity	LSB voltage of the gray scale voltage	1
V_8 to V_1	O	Open	Test pin. Set open.	1

5.10 RGB Interface Signal Pins

Table 13 RGB Interface Signal Pins

Pin Name	I/O	Connected To	Description	Number of Pins
VSYNCI	I	MPU	Vertical synchronization input pins. Enters the vertical synchronization signal when set for the VSYNC interface, RGB transfer 2 or 3 using the Set Display Data Interface command. If it is not set, no entry operation takes place. So it is possible to set it open.	1
VSYNCO	O	MPU	Vertical synchronization output pins. Outputs the vertical synchronization signal.	1
VSYNCO2	O	Open	Vertical synchronization output pins. Outputs the vertical synchronization divided into 1/2. As it is a test pin, set it open.	1
HSYNC	I	MPU	Horizontal synchronization pins. Enters the horizontal synchronization signal when set for the RGB transfer 3 using the Set Display Data Interface command. If it is not set, no entry operation takes place. So it is possible to set it open.	1
DOTCLK	I	MPU	RGB interface dot clock pin. Enters the dot clock when using the RGB interface. At the rising edge or falling edge of this signal, the RGB data entered in D0 to D17 is read. When the RGB interface is not used, it is possible to set open. When the RGB transfer 3 is set, it becomes the display reference clock signal and the reference clock of a booster clock.	1
ENABLE	I	MPU	RGB Interface enable pin. This is the data enable signal when using the RGB interface. When the RGB interface is not used, it is possible to set open.	1

5.11 LCD Output Pins

Table 14 LCD Output Pins

Pin Name	I/O	Connected To	Description	Number of Pins
S1 to S528	O	LCD	Source line drive output pins. Converts digital display data into analog form (D/A conversion) and outputs it.	528
G1 to 220	O	LCD	Gate line drive output pins. Outputs gate line selection level: V_{DDHG} and non-selection level: V_{EE}.	220
GD1 to 4	O	LCD	Dummy gate line drive output pins. Continuously outputs V_{EE} voltage level.	4
V_{COM}	O	LCD	V_{COM} signal output pin. Used as the common electrode signal for the TFT panel.	8

5.12 Test Pins

Table 15 Test Pins

Pin Name	I/O	Connected To	Description	Number of Pins
TEST1	I	GND	Test pin The customer cannot use it. Be sure to enter LOW. HIGH: Test mode (adjustment of oscillation frequency and V_{REG}) LOW: Normal operation mode	1
TEST2	I	GND	Test pin The customer cannot use it. Be sure to enter LOW. HIGH: Test mode (Built-in power output is not discharged.) LOW: Normal operation mode. (Built-in power output is discharged.)	1
TEST3	I	V_{DDI}	V_{CORE} disable pin Set HIGH when supplying an external power supply to the V_{CORE} pin. HIGH: Forcefully turns V_{CORE} OFF. (Not discharged.) LOW: Normal operation mode. (Discharge is carried out when V_{CORE} OFF.) See section 6.7 How to Connect to External Power Supply. Connect it to V_{DDI} to connect with external power supply basically.	1
TEST4	I	GND	V_{CORE} force enable pin Used to not discharge V_{CORE} in the sleep in state. HIGH: Forcefully turns V_{CORE} ON. (Not discharged.) LOW: Normal operation mode. (Discharge is carried out when V_{CORE} OFF.) See section 6.7 How to Connect to External Power Supply. Connect it to GND to connect with external power supply basically.	1
TEST5	I	GND	Test pin (The customer cannot use it. Be sure to enter LOW.) HIGH: Test mode LOW: Normal operation mode	1
TRI	O	Open	Test pin. Internal constant current adjustment pin. Fix it to open.	1
EECK	O	Open	Test pin. Fix it to open.	1
EEDA	O	Open	Test pin. Fix it to open.	1
EECS	O	Open	Test pin. Fix it to open.	1
VEP	O	Open	Test pin. Fix it to open.	1

5.13 Dummy Output Pins

Table 16 Dummy Output Pins

Pin Name	I/O	Connected To	Description	Number of Pins
DUMMY	—	Open	Dummy pin Do not connect the voltage to the DUMMY pin.	42
ADUMMY	—	Open	There are two pins that are connected by aluminum winding. When it is used, connect it within V_{SS} to V_{OUT}.	2
BDUMMY	—	Open	There are two pins that are connected by aluminum winding. When it is used, connect it within V_{EE} to V_{DDHG}.	2
CDUMMY	—	Open	There are two pins that are connected by aluminum winding. When it is used, connect it within V_{EE} to V_{DDHG}.	2
DDUMMY	—	Open	There are two pins that are connected by aluminum winding. When it is used, connect it within V_{SS} to V_{OUT}.	2

6. FUNCTIONAL DESCRIPTION

6.1 MPU Interface

This IC is provided with 8/9/16/18-bit MPU interface and 9-bit serial interface for command and display data transfer from the MPU. When you have selected the 16-bit MPU interface, you can select 2 + 16-bit or 16 + 2-bit mode using the data set command. Also, for display data transfer, 6/16/18-bit RGB interface is provided. In addition, with the VSYNC synchronization function newly provided, the system best suited to displaying both still pictures and moving pictures simultaneously can be built.

6.1.1 MPU Interface Selection

The MPU interface can be used for transferring commands and display data, and can be selected with the MPU interface select pins (IF3, IF2 and IF1) as shown in the table below.

Table 17 MPU Interface Selection

IF3	IF2	IF1	Interface	RAM Write	RAM Read
LOW	LOW	LOW	16-bit parallel	Enable	Enable
LOW	LOW	HIGH	18-bit parallel	Enable	Enable
LOW	HIGH	LOW	8-bit parallel	Enable	Enable
LOW	HIGH	HIGH	9-bit parallel	Enable	Enable
HIGH	HIGH	HIGH	9-bit serial	Disable	Disable

6.1.2 Parallel MPU Interface

Depending on the C86 pin setting, 80-series or 68-series MPU can be connected.

Table 18 C86 Test Pins

C86	$\overline{RD}$	$\overline{WR}$
HIGH: 68-series MPU bus	E	R/$\overline{W}$
LOW: 80-series MPU bus	$\overline{RD}$	$\overline{WR}$

Signals on the parallel MPU interface are identified by combination with the data/command identification pin (A0).

Table 19 MPU Interface Identification

A0	68-Series MPU		80-Series MPU		Function
	R/$\overline{W}$	E	$\overline{RD}$	$\overline{WR}$	
LOW	HIGH	HIGH	LOW	HIGH	Revision read
HIGH	HIGH	HIGH	LOW	HIGH	RAM data read
HIGH	LOW	HIGH	HIGH	LOW	RAM data, command parameter write
LOW	LOW	HIGH	HIGH	LOW	Command write

D17 to D0, DR and DB are used as 8/9/16/18-bit width bus according to the setting of the MPU interface select pins IF1, IF2 and IF3, and unused pins are set open. For commands and parameters, MSB 8 bits (D17 to D10) are used.

Table 20 MPU Parallel Interface (Except for Display Data)

Bus width	Data type	A0	Parallel MPU interface Dxx															
			17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
18-bit mode	Command	0	Command								—	—	—	—	—	—	—	—	—	—
	Parameter	1	Parameter								—	—	—	—	—	—	—	—	—	—
16-bit mode	Command	0	Command								—	—	—	—	—	—	—	—	Z	Z
	Parameter	1	Parameter								—	—	—	—	—	—	—	—	Z	Z
2+16-bit mode *	Command	0	Command								—	—	—	—	—	—	—	—	Z	Z
	Parameter	1	Parameter								—	—	—	—	—	—	—	—	Z	Z
16 + 2-bit mode *	Command	0	Command								—	—	—	—	—	—	—	—	Z	Z
	Parameter	1	Parameter								—	—	—	—	—	—	—	—	Z	Z
9-bit mode	Command	0	Command								—	Z	Z	Z	Z	Z	Z	Z	Z	Z
	Parameter	1	Parameter								—	Z	Z	Z	Z	Z	Z	Z	Z	Z
8-bit mode	Command	0	Command								Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
	Parameter	1	Parameter								Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

* 2+16bit mode and 16+2bit mode are chosen by the data set command(BCh).
— indicates invalid data.
Z indicates disable. Set the disabled pins open.

6.1.3 Serial Interface

The serial interface supports 9-bit mode. The 9-bit mode consists of three lines: chip select ($\overline{CS}$), serial clock (SCL), and serial data input (SI). When the serial interface is selected, data can be input/output by clocks while the chip is active ($\overline{CS}$=LOW). Data is transferred in the unit of 9 bits. At input, data is read in order from MSB at the clock rising edge. MSB is the data/command identification data (D/C) equivalent to the A0 signal of the parallel interface. It is the command when set to "0" and the parameter when set to "1".
To prevent malfunction due to noise, it is recommended to set the $\overline{CS}$ signal to HIGH every 9 bits. (The serial counter is reset at the falling edge of the $\overline{CS}$ signal.)

Table 21 9-bit Serial Interface (Except for Display Data)

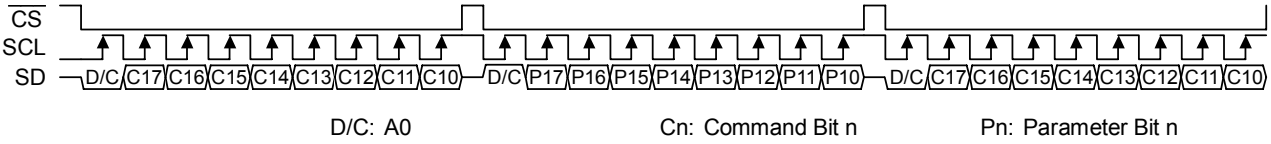
Data type	Serial interface bit position								
	DC	17	16	15	14	13	12	11	10
Command	0	Command							
Parameter	1	Parameter							

D/C: Data/command identification bit
— indicates invalid data.

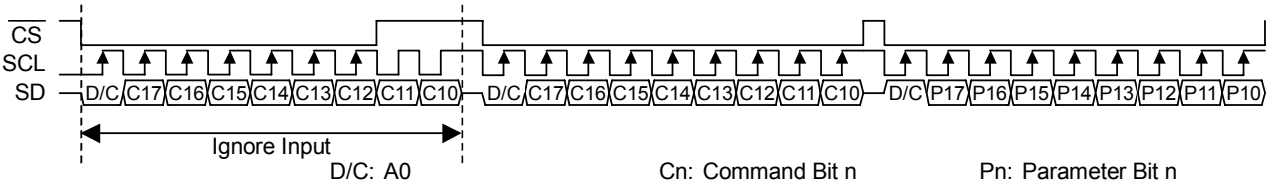
Processing starts when the serial transfer clock D10 LSB is input. Writing to or reading from the display data RAM is disabled. If any parameter exceeding the number of parameters defined for each command is entered, it is invalid.

The interface examples are given below. (The intermediate level of SD in the following diagram indicates the state of high impedance.)

◇ When writing

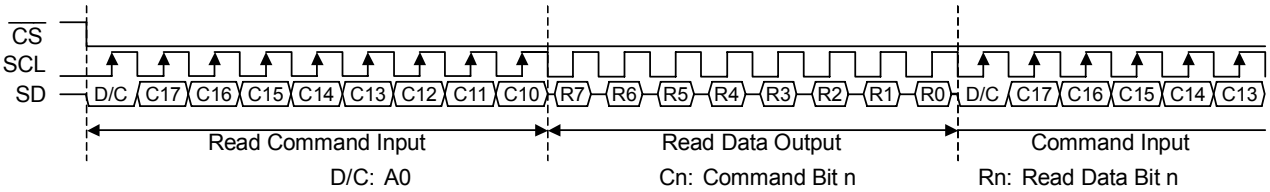


The 9-bit serial data (1 packet) must be kept at the LOW level during transfer. When $\overline{CS}$ sets to LOW, SCL should be in the state of LOW. If $\overline{CS}$ is set HIGH during 1-packet transfer, the packet in the process of transfer is cancelled. Setting LOW for $\overline{CS}$ again brings the state of accepting retransfer of the packet.

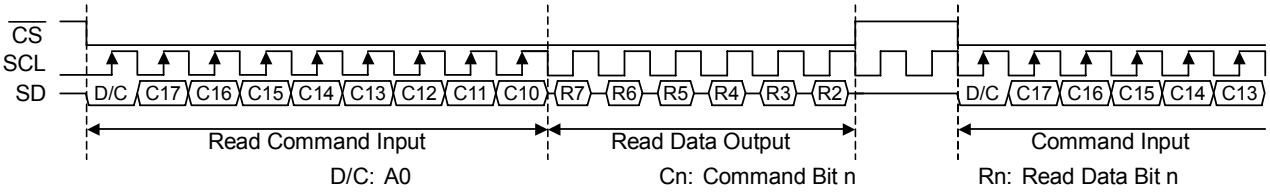


◇ When reading

When data is read using the status read and revision read commands, the following situation occurs. When $\overline{CS}$ sets to LOW, SCL should be in the state of LOW. When transfer of read data up to final bit is completed, the internal process exits the read state to the state of accepting commands.



If $\overline{CS}$ is set HIGH during read data transfer, the read state is cancelled. Setting LOW for $\overline{CS}$ again brings the state of accepting commands.



SCL pin should be LOW state, when CS is changed to LOW.

6.1.4 Internal Data Bus Expansion of Display Data

Display data read or written in the parallel MPU interface is expanded to 18-bit internal data bus and RGB data as shown in the table below.
For display data transfer in 8-bit, 9-bit, 2 +1 6-bit or 16 + 2-bit mode, two accesses are needed for a single dot. Write operation to the display RAM is executed when the second data has been transferred. Therefore, be sure to transfer data twice at a time. Otherwise, the data last transferred is not written to the display RAM. The data count is reset at RAM Write or RAM Read command identification.

Sequence of transfer from external data bus to internal data bus

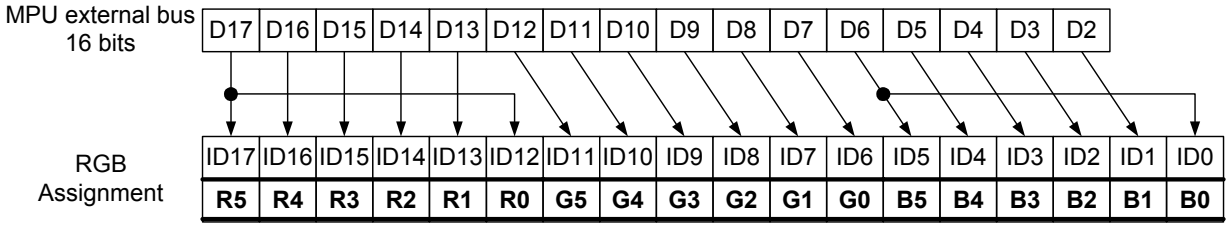


Fig.5 Parallel MPU Interface External Data Bus 16 bits

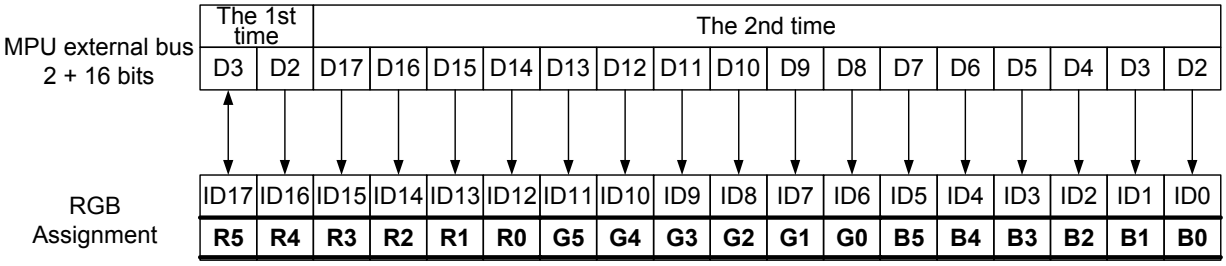


Fig.6 Parallel MPU Interface External Data Bus 2 + 16 bits

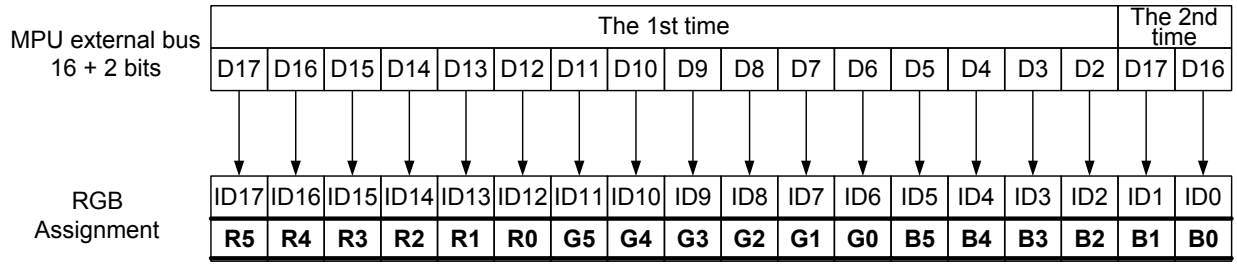


Fig.7 Parallel MPU Interface External Data Bus 16 + 2 bits

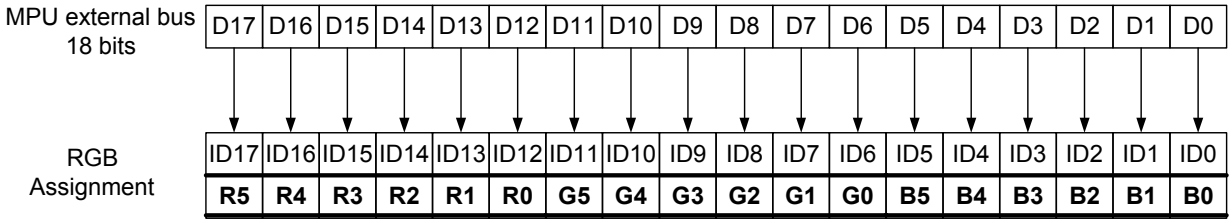


Fig.8 Parallel MPU Interface External Data Bus 18 bits

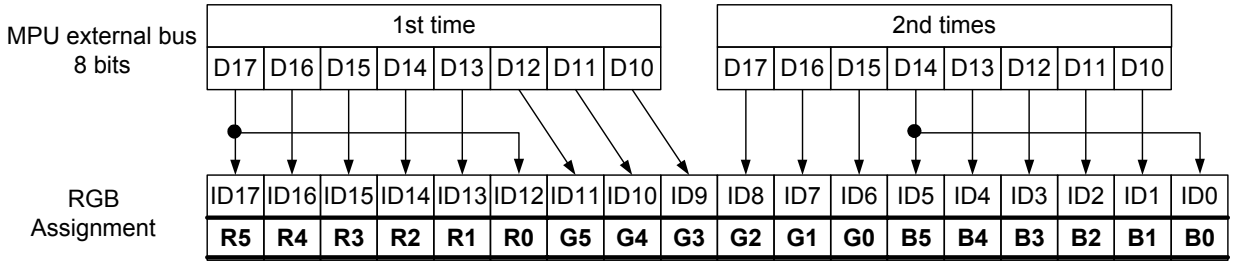


Fig.9 Parallel MPU Interface External Data Bus 8 bits

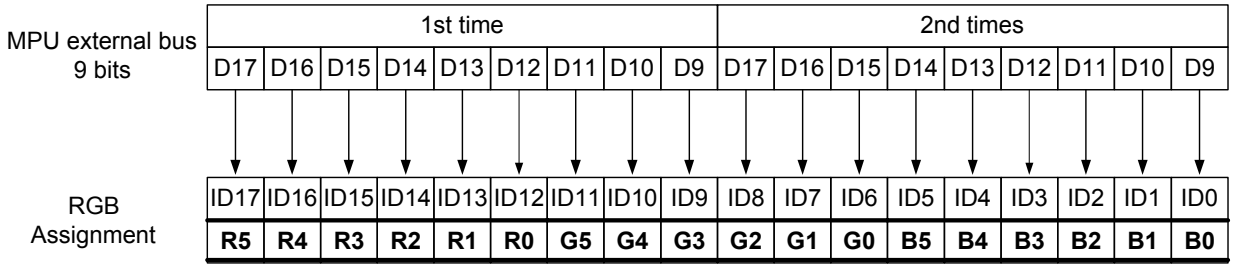


Fig.10 Parallel MPU Interface External Data Bus 9 bits

6.1.5 Access to Display Data RAM and Internal Register via MPU Interface

When data is transferred to or from the MPU, a kind of pipeline operation is performed, generating the internal pulse for each access. Therefore, access from the MPU does not require the reference clock, providing low power consumption. Also, an access succeeds if it ends within the cycle time. No weight is required and high-speed data transfer can be realized.

For example, when the MPU writes data to the display data RAM, the data is temporarily held by the write bus holder. Then, it is written to the internal RAM with the internal pulse (Write signal) by the time the next Write Data cycle starts. Also, when the MPU reads display data in the internal RAM, the data is read in the first Read data cycle (dummy) and is held by the read bus holder with the internal pulse (Read signal), then the data is read in the system bus from the read bus holder in the next Read data cycle.

A single dummy read is always required after the Read command.

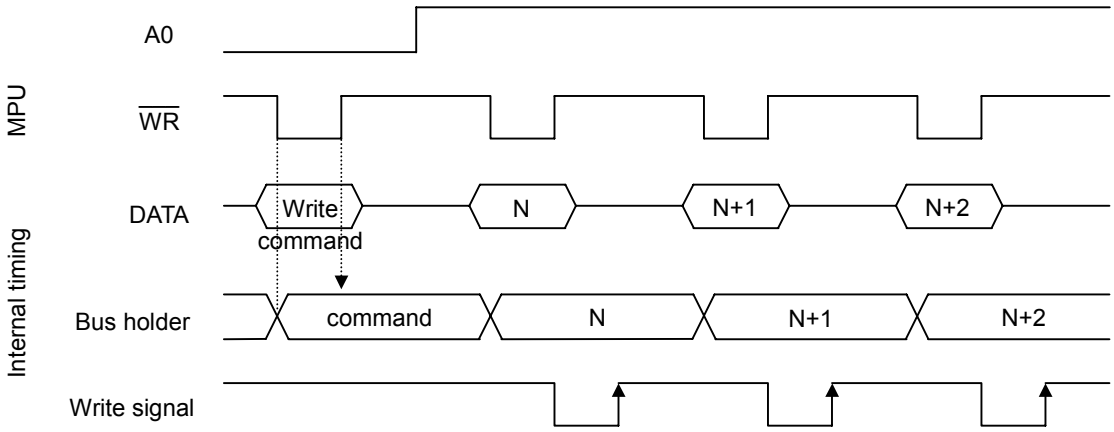


Fig.11 MPU Interface Write Operation Example

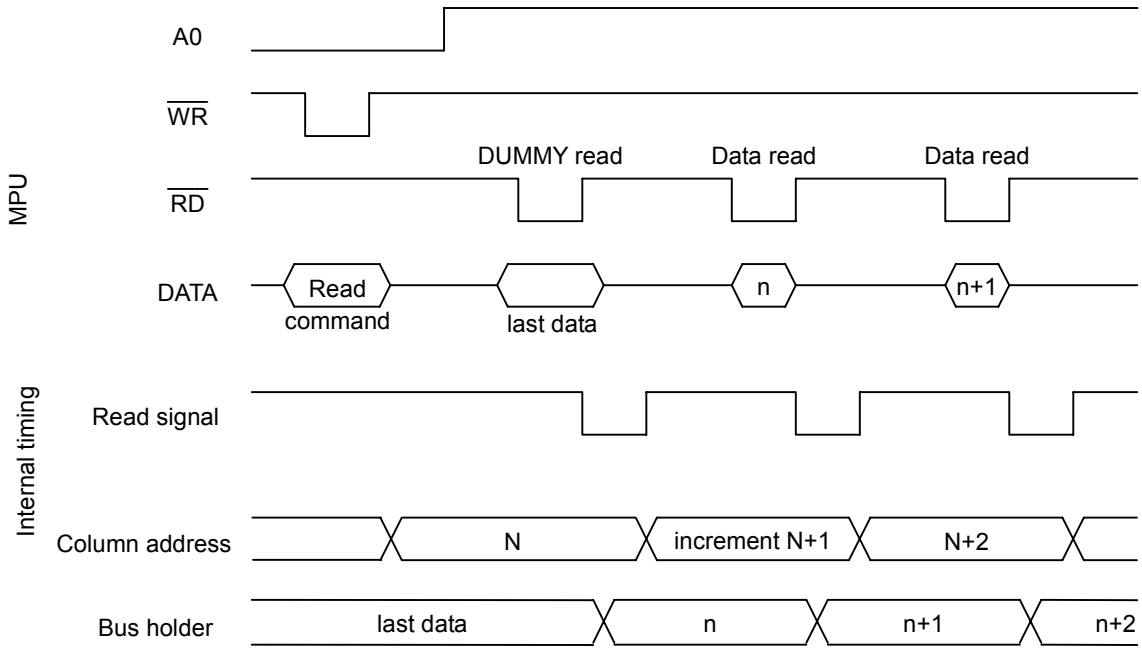


Fig.12 MPU Interface Read Operation Example

6.1.6 VSYNC Interface

The VSYNC is included as the means of smoothly displaying moving pictures while using the MPU interface. Moving pictures can be smoothly displayed without using the RGB interface.
In the VSYNC interface, the display timing is determined by the built-in oscillation clock and frame synchronization signal (VSYNCI). If VSYNC is not entered, all the display timings are determined by the built-in oscillation clock. Once VSYNCI is entered, however, the display timing synchronizes with VSYNCI and it is set at the head (the first line of the back poaching) of a frame. The RAM address (column address and row address) is also set to the start address.
To obtain smooth moving pictures on the moving picture display, relationship between the lower limit of the RAM read speed and built-in oscillation clock must be considered.
To prevent display distortion, the display RAM write operation must be performed at the speed high enough not to be passed by the relevant line data read operation speed at the display timing. See also section 6.3 Write Speed to Display Data RAM.

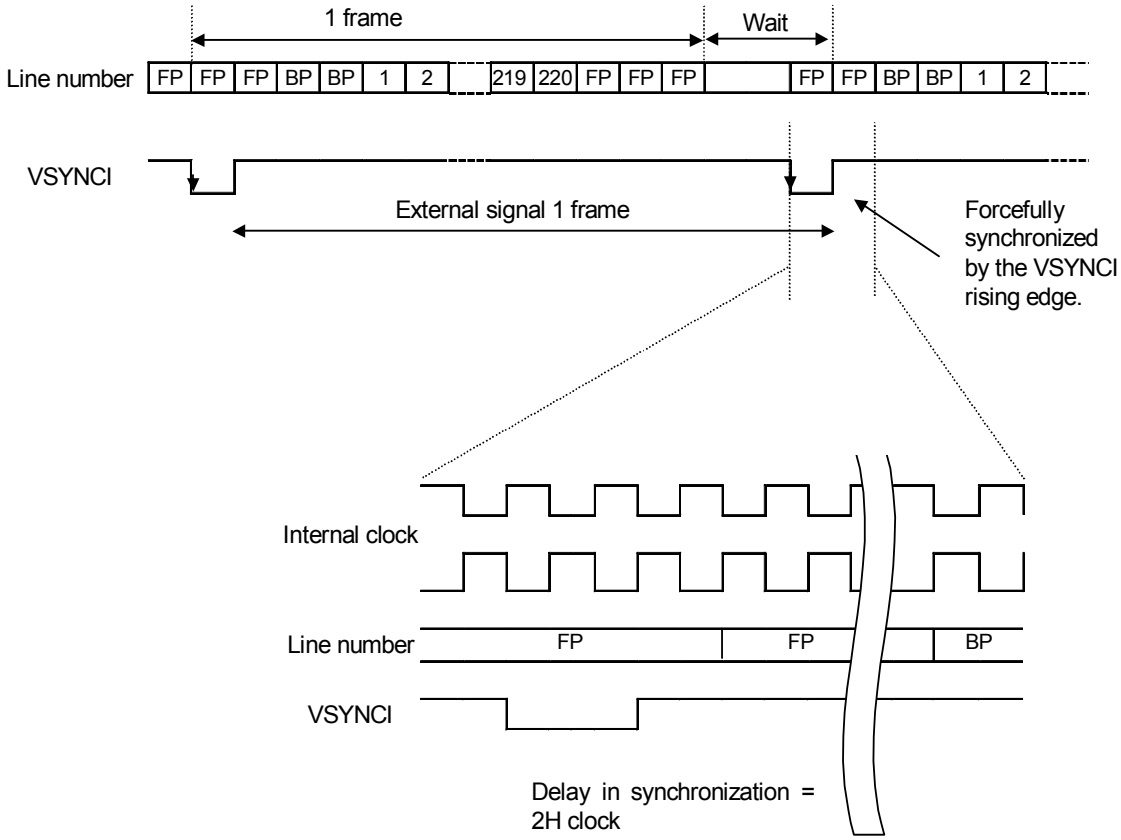


Fig.13 VSYNC Interface Example

6.2 RGB Interface

This IC is provided with the RGB interface best suited to displaying moving pictures, in addition to the MPU interface used to connect to the MPU. As with the MPU interface, the display RAM write address is a rectangle area defined by the Set Start Address and Set End Address commands.
Only the display RAM write operation is enabled via the RGB interface Command input, display RAM read or status read operations are disabled. Command access from the MPU interface can be accepted at any time. However, those commands accessing the display RAM (RAM Write, RAM Read and Read Modify Write) cannot be entered. Be sure to perform the operation after access via the RGB interface has been completed.

6.2.1 RGB Interface Selection

The RGB interface bus width can be selected according to the settings of the Set Display Data Interface command parameter as shown below.

Table 22 RGB Interface Selection

P15	P14	RGB interface bus width
0	0	18-bit, transfer once
0	1	16-bit, transfer once
1	0	6-bit, transfer three times
1	1	Setting disabled

6.2.2 RGB Interface Operation Modes

By setting the RGB interface status using the Set Display Interface command, the best suited interface to the display status can be used for data transfer to the display RAM.

Table 23 RGB Interface Operation Modes

Data transfer mode	Display timing Reference clock	DOTCLK	ENABLE D17 to 0	VSYNCI	VSYNCO	HSYNC
RGB transfer 1	Internal oscillation	Valid	Valid	Invalid	Valid	Invalid
RGB transfer 2	Internal oscillation	Valid	Valid	Valid	Valid	Invalid
RGB transfer 3	DOTCLK	Valid	Valid	Valid	Valid	Valid

RGB transfer 1

To write data to the display RAM, access it using D17 to 0, ENABLE and DOTCLK.
As timing signals necessary for display operation, the signals generated inside the IC are used.
Since vertical synchronization signals generated in the internal timing are output from the VSYNCO, flicker-free display is achieved by transferring the display data from the RGB interface synchronizing with these signals.

RGB transfer 2

To write data to the display RAM, access it using D17 to 0, ENABLE and DOTCLK.
As timing signals necessary for display operation, internal signals of the IC are used. These signals are forcedly synchronized with the frame top by VSYNCI entered externally. Set the RAM address to the start address. VSINCI must be continuously supplied externally.

VSYNCI must be entered during the period of front poaching (FP).

RGB transfer 3

To write data to the display RAM, access it using D17 to 0, ENABLE and DOTCLK.
As timing signals necessary for display operation, all the external signals are used. VSYNCI, HSYNC and DOTCLK must be continuously supplied externally. The RAM address is set to the start address by the VSYNCI input.

If DOTCLK is faster than the clock frequency (1MHz) of the built-in oscillation circuit, it is recommended to set to the value close to 1MHz by dividing DOTCLK by P2 of the display data interface set. Division is valid only for the clock used for the display timing (to reduce current consumption). Write clock to RAM is not divided.

To switch from the MPU interface to RGB transfer 3, the following command must be set according to the display timing externally entered.

Display set (command code: CAh)

P1 and P2	Number of clocks during 1H	It is set as the short number of clocks more than the number of 1 clocks rather than the cycle of HSYNC. (Used for calculation of frequency setting of the boosting clock set at P4. If the cycle changes, set in the shortest cycle.)
P7	Number of back poaching line (BP)	Set the value longer than the timing at which write to RAM starts.

Display timing set (command code: A1h)

P1 to P4, P6 and P7	Various timings	It is set as the number of clocks of DOTCLK within the number of clocks of 1H set up by the display set. (When dividing, the clock after dividing is reference clock.)

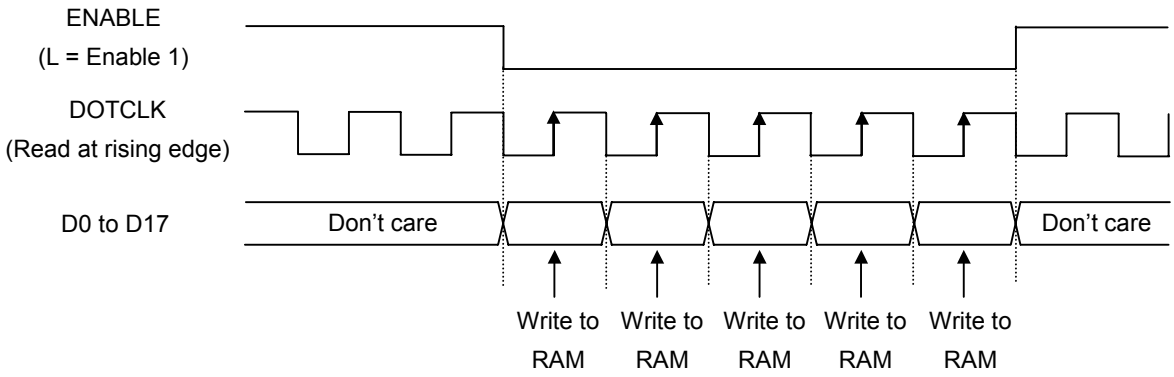


Fig.14 Write to RAM (Common to RGB transfer 1 to 3)

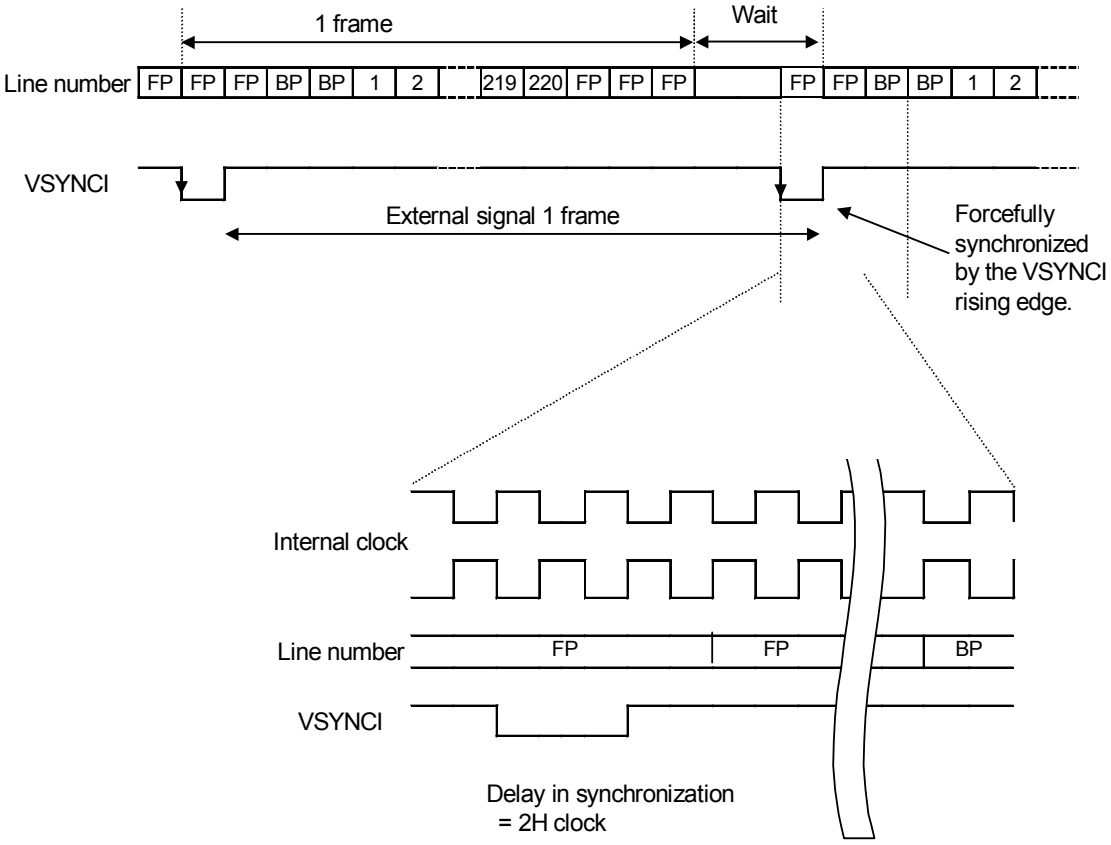


Fig.15 Example of RGB Transfer 2 (VSYNC Synchronization)

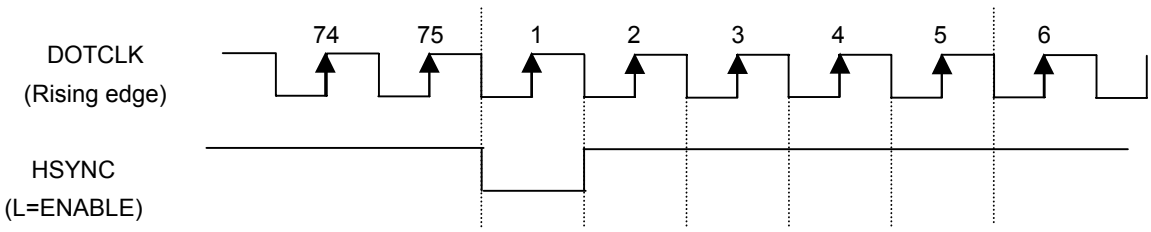


Fig.16 Example of RGB Transfer 3 HSYNC and DOTCLK timing

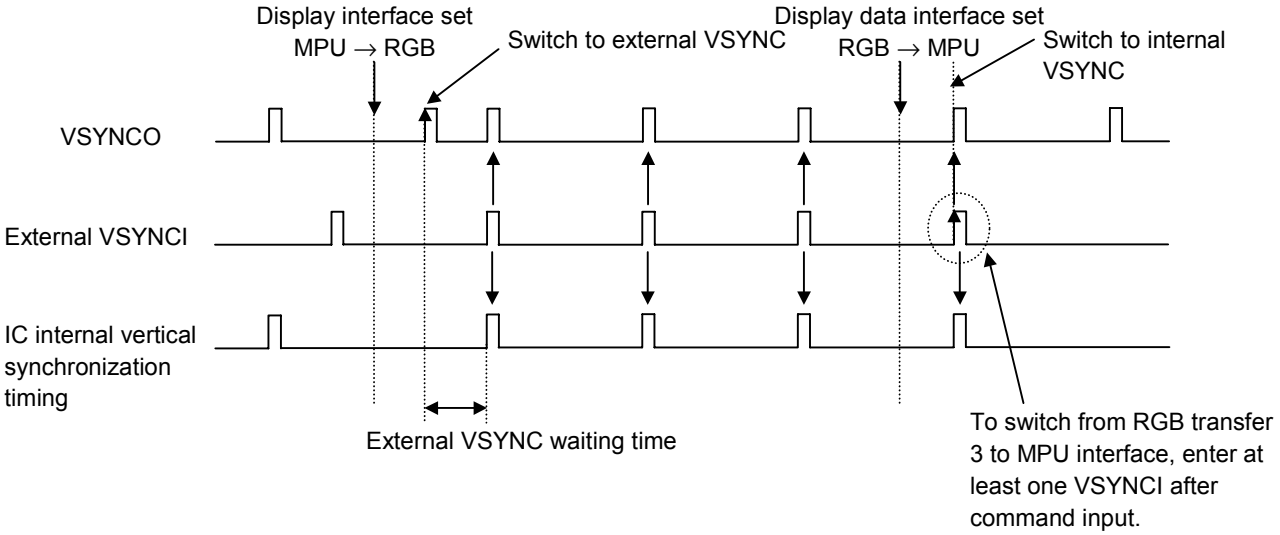


Fig.17 Example of Switching Display Timing between RGB Transfer 3 and MPU Interface

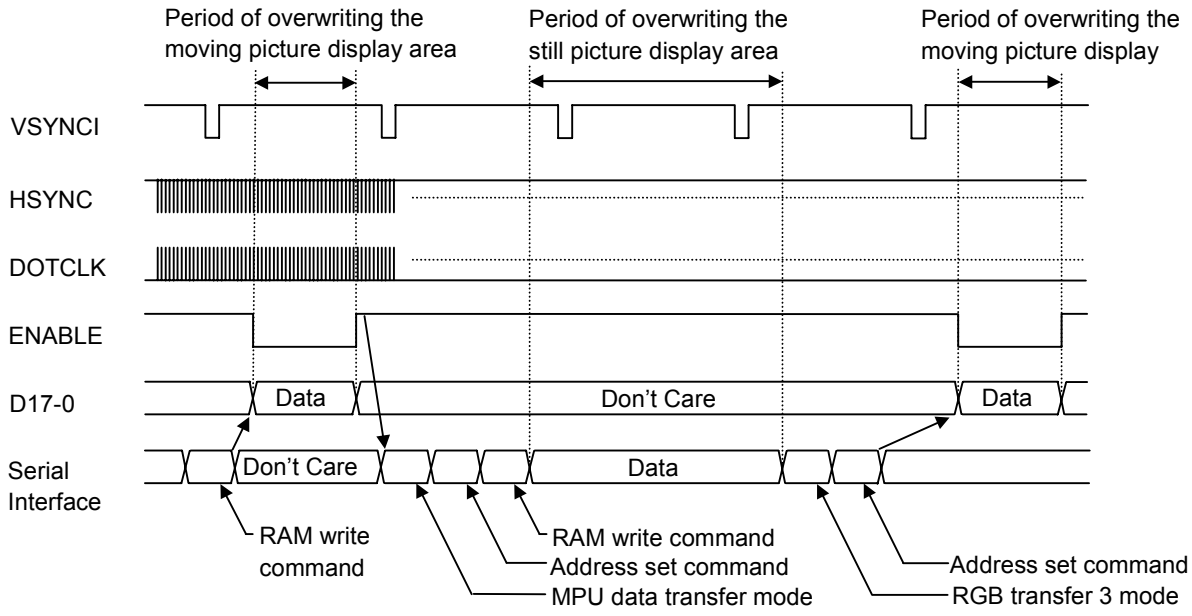


Fig.18 Example of Overwriting the Still Picture Display Area During Moving Picture Display Operations

6.2.3 Internal Data Bus of RGB Interface

Data entered from the RGB interface data pin is read by DOTCLK as display data.

The display data is expanded into the 18-bit internal data bus as shown below. In 6/16-bit mode, set unused pins to open.

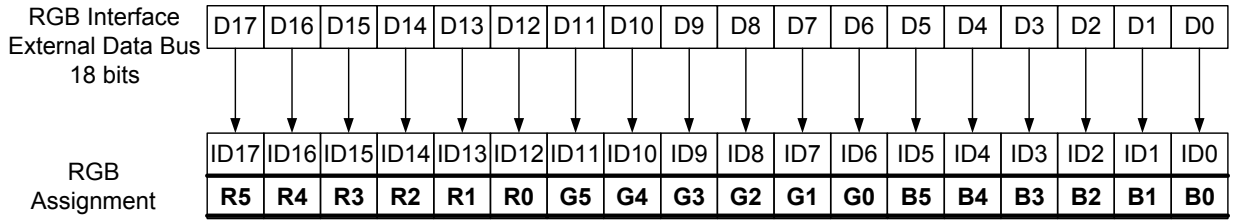


Fig.19 RGB Interface External Data Bus 18 bits

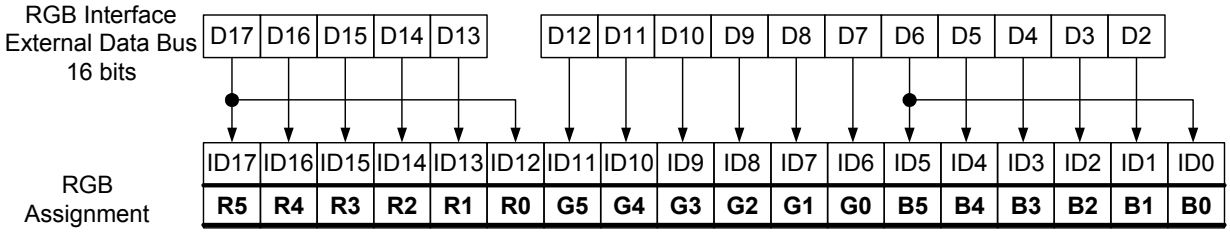


Fig.20 RGB Interface External Data Bus 16 bits

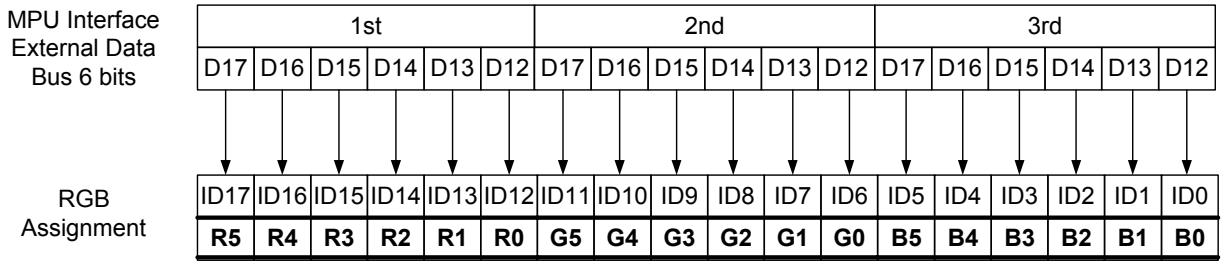


Fig.21 RGB Interface External Data Bus 6 bits

6.2.4 Access to Display Data RAM via RGB Interface

With the RGB interface, the display data is read and written to the built-in display RAM at the rising edge of DOTCLK signal. DOTCLK and ENABLE are used for writing to the display RAM. In the 16/18-bit mode, a single dot is read at a time. In the 6-bit mode, a single dot is read as the display data in three steps, in the order of R, G and B. By combining with the wind address, display data in a rectangle area can be transferred. The display RAM data and addresses are updated only while the ENABLE signal is LOW. When using the RGB interface, scroll display function is available. But it does not recommend using. Because the reading order to the internal RAM changes writing data is passed to the reading of the internal RAM and the image sometimes scrambles.

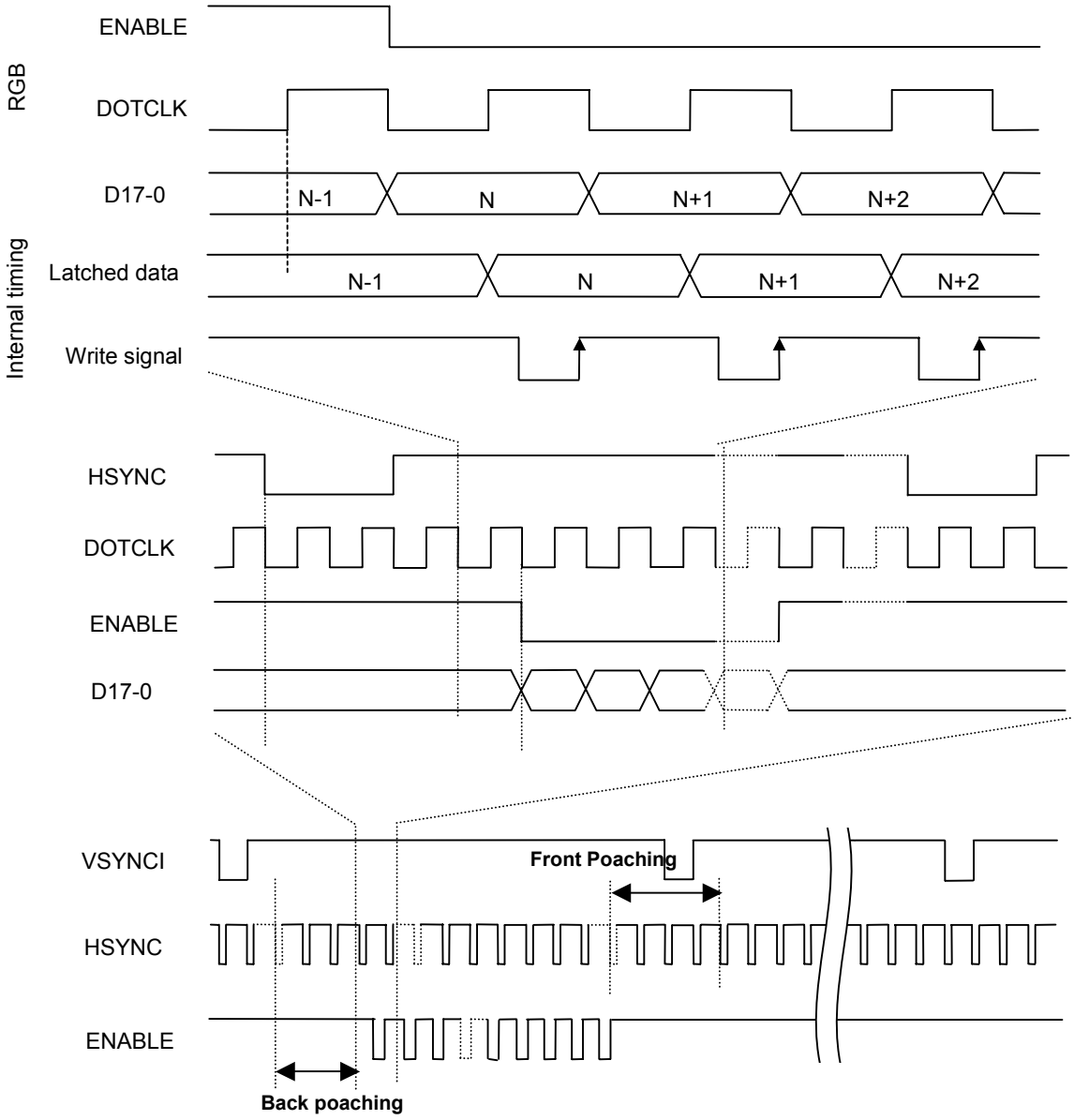


Fig.22 Example of Writing Data into Display Data RAM

When using the RGB interface, back poaching starts after 2H from the falling edge of VSYNCI, and then display operation is performed. After the display operation, front poaching is performed. Front poaching can be set to 1 to 4096. Back poaching can be set to 1 to 256.

In case of VSINCI is Low enable; raising edge sets RAM address. In case of VSINCI is High enable; falling edge sets RAM address. Then RAM writing should start after it.

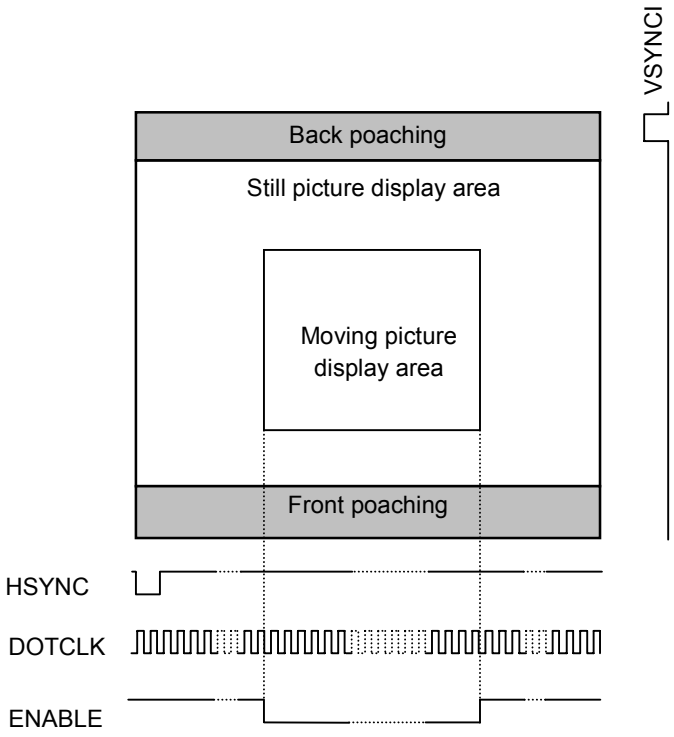


Fig.23 Moving Picture and Still Display Area

6.3 Write Speed to Display Data RAM

In moving picture display via VSYNC interface, RGB transfer 1 or RGB transfer 2, the display RAM write operation must be performed at a speed not to be caught up by the line data read operation speed at display timing to prevent display distortion. When the back poaching is not specified, even if the RAM write operation is performed at a high speed, it is caught up with by the display timing in the first line. Specify back poaching of 2 lines or more. Please pay attention because the following calculation is not able to apply in the case that the scrolling function is used.

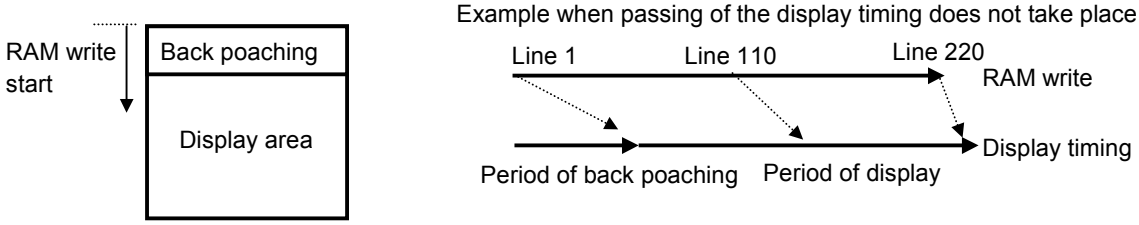


Fig.24 Write Speed to Display Data RAM

The display data must be written to RAM at the speed faster than that calculated from the relational expression shown below.

Number of clocks in 1H =
(1 /((Number of display lines + back poaching + front poaching) × Number of frame frequency / Oscillation frequency)

$$\text{Minimum RAM write speed} > \frac{176 \times \text{Number of display lines}}{(\text{Number of display lines} + \text{Back poaching}) \times \text{Number of clocks in 1H} \times 0.9\mu s - \text{Start time of write operation from VSYNCO or VSYNCI}}$$

An example of setting the RAM write speed based on the above relation expression is given below.

Number of display lines: 220 lines
Back poaching: 15 lines
Front poaching: 4 lines
Number of data in 1H: 176 (when using 16/18-bit bus)
Start time of write operation from VSYNCO or VSYNCI: 20µs
Oscillation frequency: 1MHz ±10% (oscillation frequency 1µs ±10%)
Frame frequency: 60Hz

Number of clocks in 1H =

(1 / ((220 +15 + 4) × 60Hz)) / 1µs = 69.7 So, it makes 70 clocks.

To make RAM write completion time < Display read completion time true.

$$\text{Write speed} > \frac{176 \times 220}{(220 + 15) \times 70 \times 0.9\mu s - 20\mu s} \fallingdotseq 2.62\text{MHz}$$

Therefore, for write operation at 2.62MHz or over, screen distortion can be eliminated.

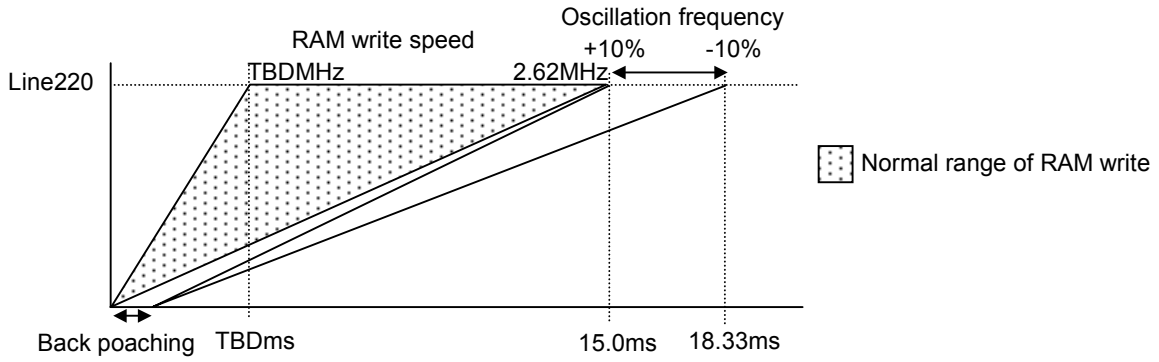


Fig.25 Write Speed to Display Data RAM

Start the writing to RAM after a back porch period start. Cautions, a start address is reset at the time of a front porch and a back porch change.

6.4 Display Data RAM

6.4.1 Display Data RAM

RAM that stores dot data for display. One dot consists of three dots (R, G and B), and one dot holds 6-bit display data. 18 bits of the internal data bus correspond to R dots (R5, R4, R3, R2, R1 and R0), G dots (G5, G4, G3, G2, G1 and G0) and B dots (B5, B4, B3, B2, B1 and B0). Maximum display size is 176 × 220 dots and the RAM capacity is 696,960 bits (176 × 220 × 18). Correspondence between display data and gray scale are shown.

(000000): Gray scale 0 (0%, black) Normally white liquid crystal V_{COM} = LOW
(000001): Gray scale 1
:
(111110): Gray scale 62
(111111): Gray scale 63 (100%, RGB)

Table 24 Display Data Memory Map

Row Address		Dot										Line
Normal	Reverse	R	G	B	R	G	B		R	G	B	Address
0	219	R5 to R0	G5 to G0	B5 to B0								0
1	218											1
218	1											218
219	0											219
Column Address	Normal	0			1				175			
	Reverse	175			174				0			
		S1	S2	S3	S4	S5	S6		S526	S527	S528	

The MPU and RGB interfaces access the display RAM in the unit of one dot. To the source output, at the internal display timing independent of the MPU or RGB interface, display data read for each line specified with line address for line cycle is sent.

Normal or reverse setup of row and column addresses are specified with the Set Data command parameters.

6.4.2 Source Line Drive Output Pins and RAM Data

The output destination of R, G and B dot data of display data RAM can be switched by the Set Data command according to the LCD color filter layout.

Table 25 Source Line Drive Output Pins and RAM Data

Output pin	S1	S2	S3	S4	S5	S6	•••	S528
Normal	R	G	B	R	G	B	•••	B
Reverse	B	G	R	B	G	R	•••	R

6.4.3 Row Address Circuit/Column Address Circuit

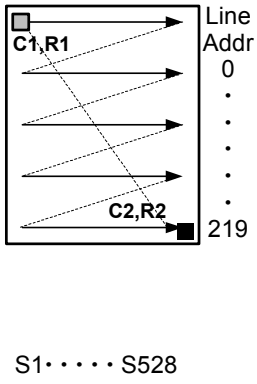
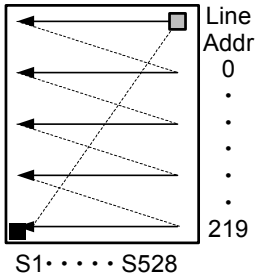
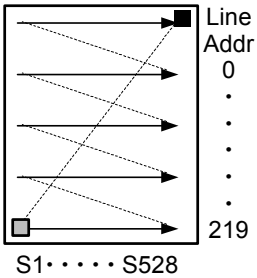
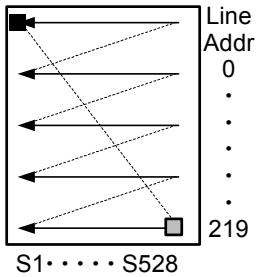
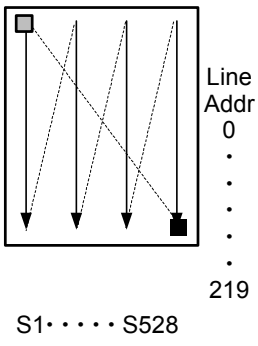
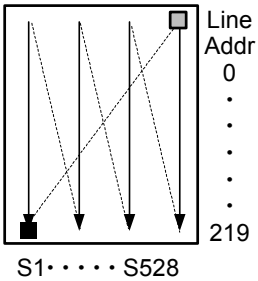
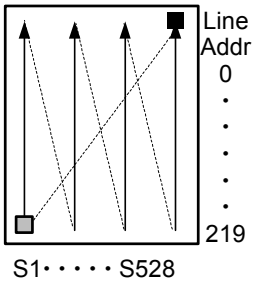
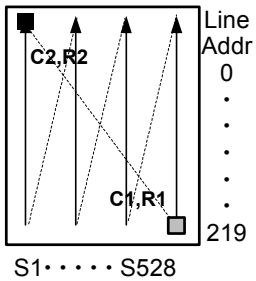
An access area of the RAM is defined by a rectangle having the vertex identified by the start address and end address. Assume that the start address has column address C1 and row address R1, and that the end address has start address C2 and row address R2. The display data is written in address (C1, R1) and subsequent addresses, and if the address is in the column direction, the column address is incremented by +1 automatically for each Write or Read pulse. After the data has been written in column address C2, the row address is incremented by +1 and the column address is returned to C1. After the end address of (C2, R2) has been written, it is returned to the start address.

During the RAM access via the MPU interface, when a RAM Write command or RAM Read command is entered, the column and row addresses are set to the start address automatically.

During the RAM access via the RGB interface, the column and row addresses are set to the start address automatically at the beginning of the frame (VSYNC timing).

The address direction of a column or a row address and the address scan direction can be inverted by Set Data command.

Table 26 Row /Column Display Sequence

Address transition Display start position C1,R1 ■ Display end position C2,R2 ■	**P10=0 Row address normal**		**P10=1 Row address reverse**	
	P11=0 Column address normal	**P11=1 Column address reverse**	**P11=0 Column address normal**	**P11=1 Column address reverse**
P13=0 Scan direction right and left				
P13=1 Scan direction up and down				

6.4.4 Area Scrolling

The RAM can be divided into a maximum of three sections in the row direction and the fixed display and scrolling areas can be created.

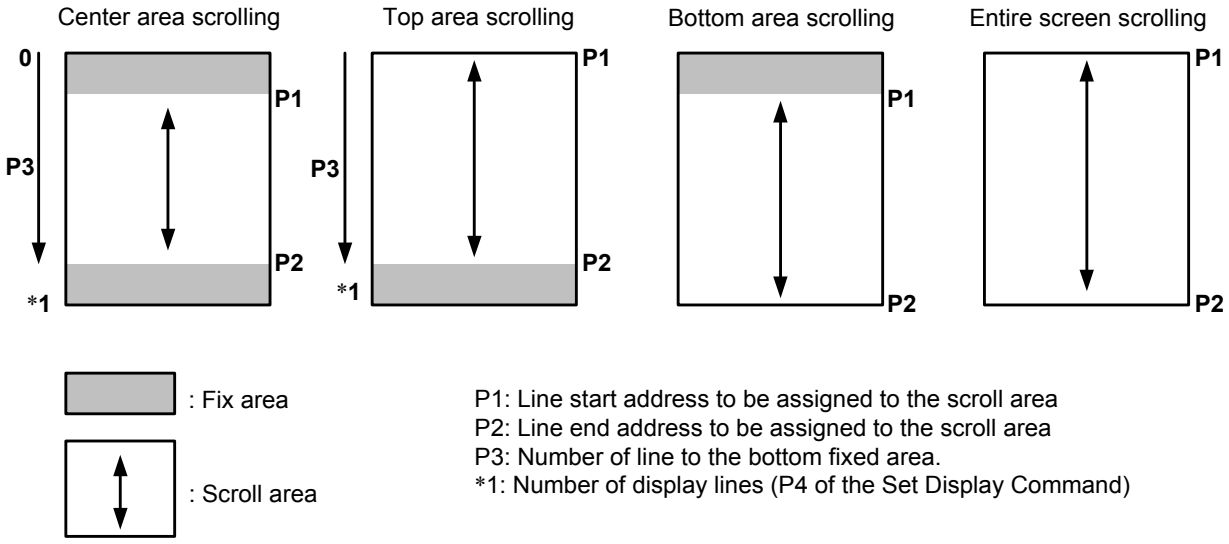


Fig. 26 Area Scrolling

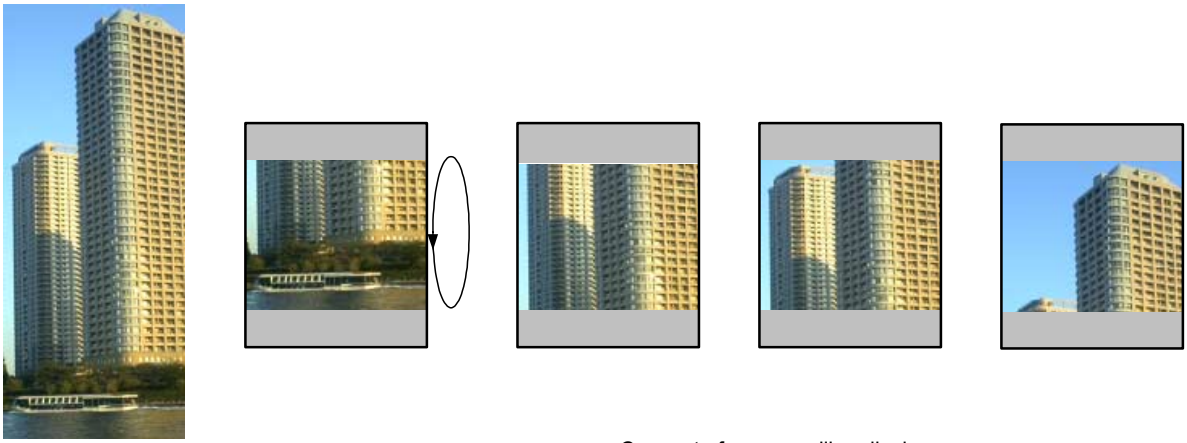


Fig.27 Concept of Area Scrolling Display

6.4.5 Partial Display

When the RAM display area is specified by the Partial Display In command, partial display areas consisting of any number of lines can be created in any position of the LCD screen. The source line drive waveforms of the RAM data appear within the partial display area, while minimum voltage level (V_0, V_{63}) output against the V_{COM} signal or power supply voltage of V_{DDHS}/V_{SS} in the non-display area. In the non-display area, power consumption can be reduced in proportion to the number of non-display lines to stop circuits that generates gray scale voltage. By specifying the 8-color mode, power consumption can also be reduced. By selecting the refresh rate of a non-display area the further low power is possible. It is possible to set the power supply control of the term that does not do the refreshing of a non-display area in detail with a partial power control. By setting an display area to 8 color modes and the reduction of the consumption power be possible.

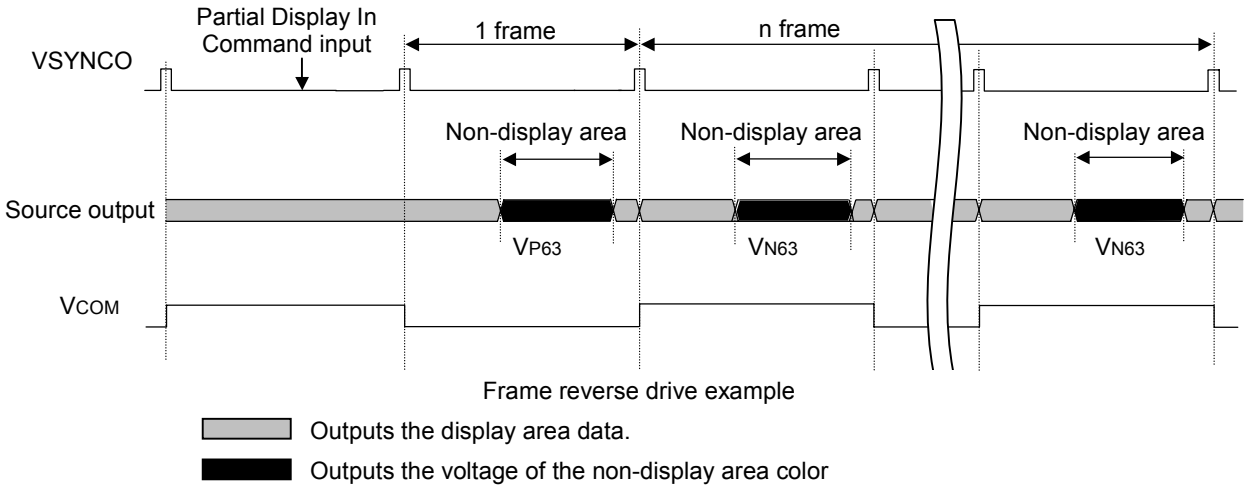


Fig.28 Partial Display (refresh rate 1/1)

The driving method of front poaching period(FP) and back poaching period(BP) during partial display are as follows. The front poaching becomes being the same as that of a non-displaying area. The back poaching becomes being the same as that of display area.

6.4.6 AC Operation Drive

With this IC, the following AC operation modes can be used.

(1) Frame reverse driving: Reverses the AC operation signals once for each frame.
(2) n-line reverse driving: Reverses the AC operation signals for every 1 to 16-line frame display.
(3) Interlace drive: Reverses the AC operation signals three times for each frame with 3-line interlace drive.

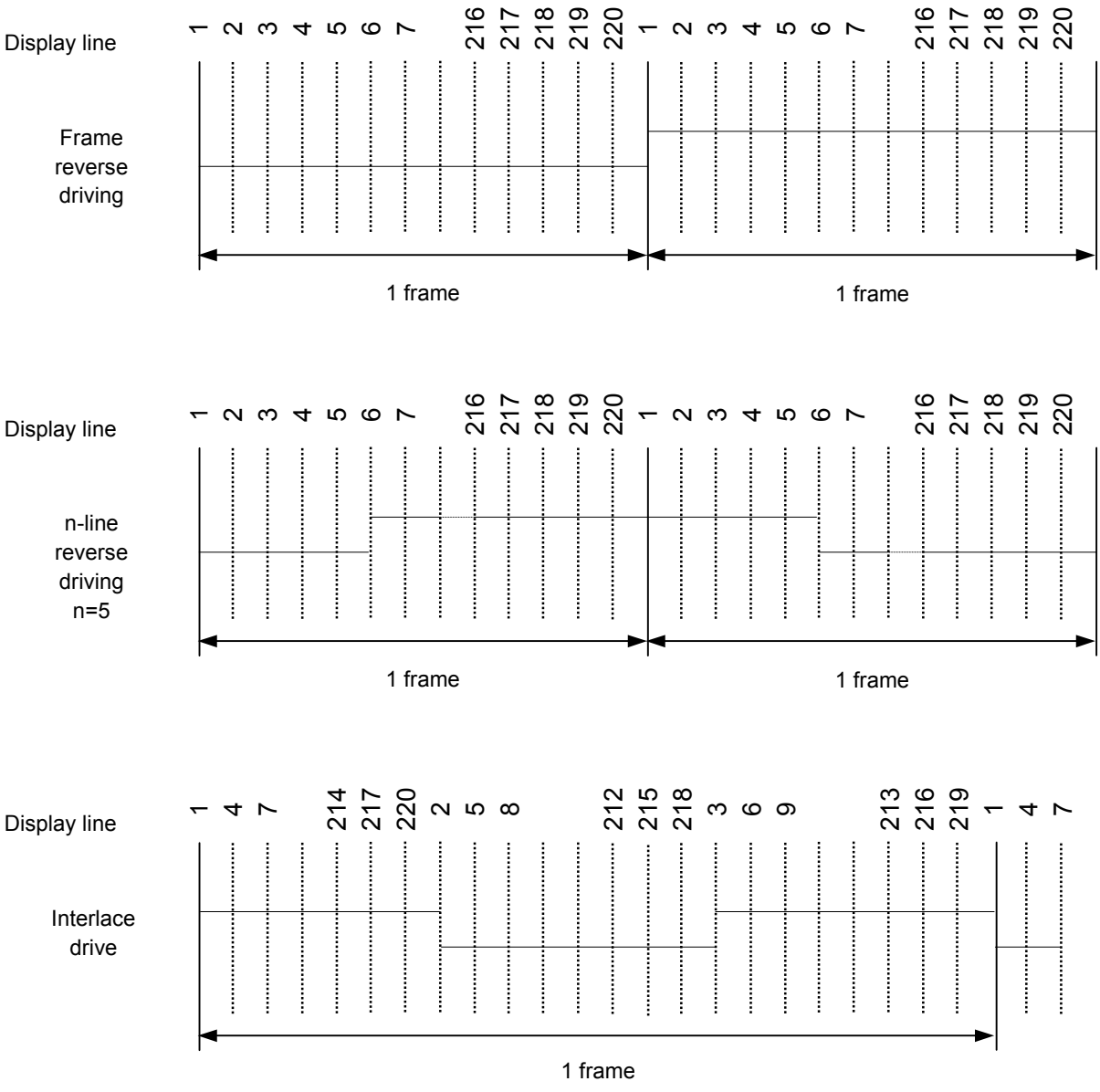


Fig.30 AC Operation Drive

6.5 Oscillation Circuit

This is a fully built-in CR-type oscillator to generate display clocks. The oscillation starts when the sleep state is canceled by the Sleep Out command. The oscillation stops when the sleep state is set by the Sleep In command.
When it is set by the Set Data command P17 that the built-in oscillator is not used, the oscillation circuit does not function. In such a case, the OSCI pin functions as the input pin of external clocks.

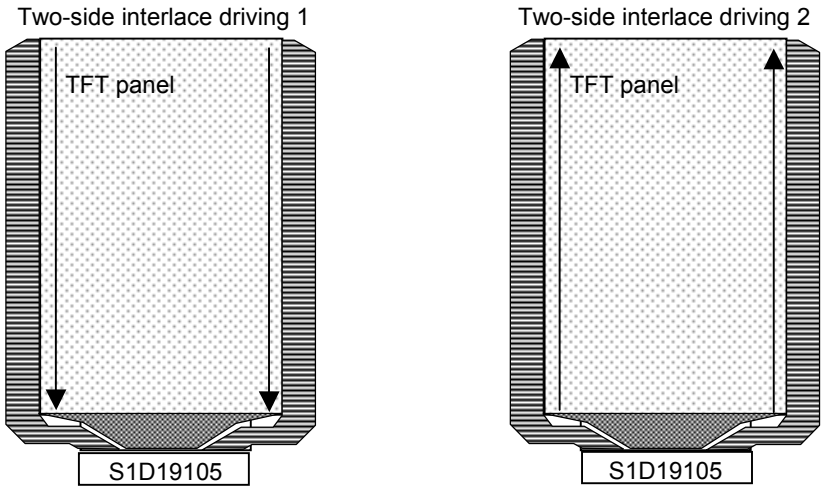
6.6 Setting Gate Line Scan Mode

You can select two-side driving or two-side up and down driving.
The drive mode is specified with the Set Gate Line Scan Mode command parameter. Set the gate driver scan start and end lines. There is a gate line of a maximum of 220 lines. And the gate line of 110 lines is in right and left. When using it by less than 220 lines, it assigns equally (right and left of the number of use lines) from G110 pin G111 pin most located in the middle. The number of lines on either side is surely made the same.
The value set up in Gate Line scan mode set is the output signal of a gate driver, and is the gate line number which begins from G1. The gate line number at the very end of the use line continuously assigned from G110 pin G111 pin is set up. Please take care that this is not a line address. And the number of display set of P5(number of dots) and the number of use lines need to be completely in agreement.

Setting example:
Conditions is P5 of display set (number of dots) = 208 line

The number of use lines of one side =208/2=104 lines
Scanning start line number =111-104=7
Scanning end line number =110+104=214

Regardless of interlace driving and Two-side up and down driving 1/2, it becomes like the above-mentioned example of calculation.

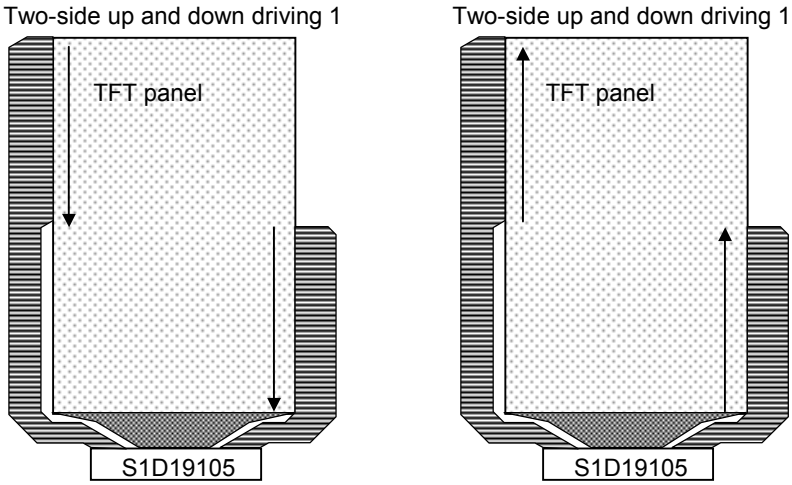


	Scan order
Normal direction	G1→G220→G2→G219→・・・→G110→G111
Reverse direction	G111→G110→G112→G109→・・・→G220→G1

220-line display example: Start line = 1, end line = 220

	Scan order
Normal direction	G11→G210→G12→G209→・・・G110→G111
Reverse direction	G111→G110→G112→G109→・・・G210→G11

200-line display example: Start line = 11, end line = 210

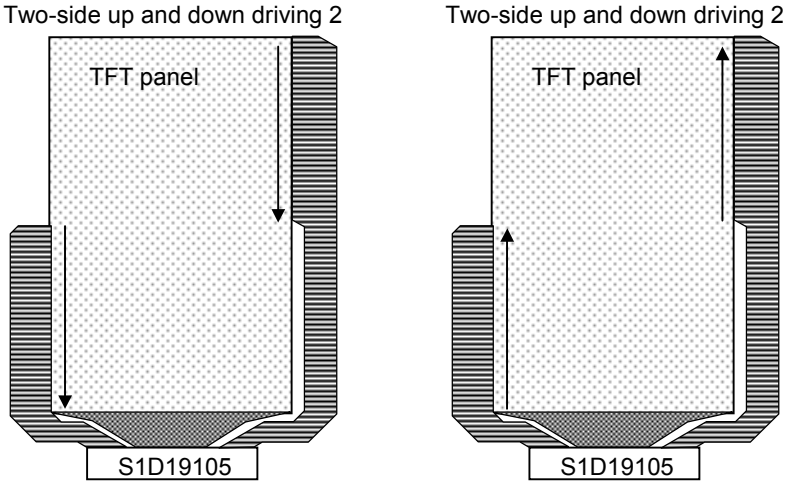


	Scan order
Normal direction	G1→G110→G220→G111
Reverse direction	G111→G220→G110→G1

220-line display example: Start line = 1, end line = 220

	Scan order
Normal direction	G11→G110→G210→G111
Reverse direction	G111→G210→G110→G11

200-line display example: Start line = 11, end line = 210



	Scan order
Normal direction	G220→G111→G1→G110
Reverse direction	G110→G1→G111→G220

220-line display example: Start line = 1, end line = 220

	Scan order
Normal direction	G210→G111→G11→G110
Reverse direction	G110→G11→G111→G210

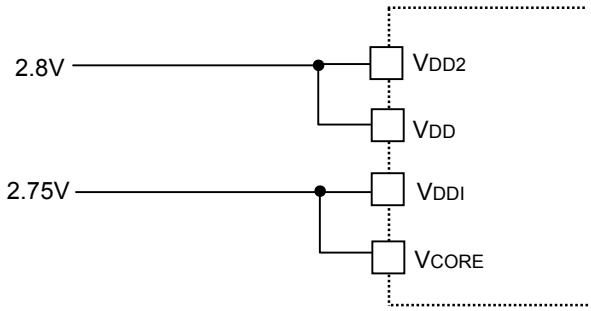
200-line display example: Start line = 11, end line = 210

Fig.31 Gate Line Scan Mode

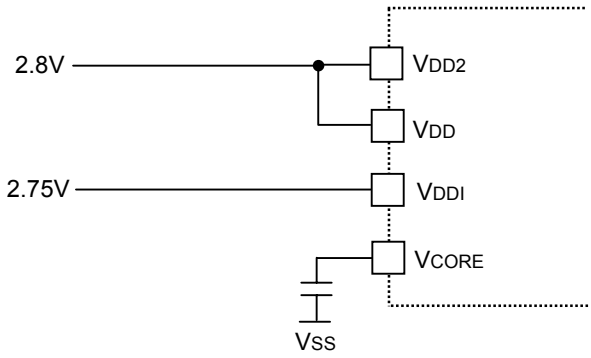
6.7 How to Connect to the External Power Supply

Case (1) Two power supplies (2.3V or more)
(Example AV_{DD} = 2.8V, DV_{DD} = 2.75V)

TEST3=H TEST4=L (V_{CORE} is normally OFF) : This connection should be used basically.



TEST3=L TEST4=H (V_{CORE} is normally ON)



TEST3=L TEST4=L (V_{CORE} automatic stop, automatic start)

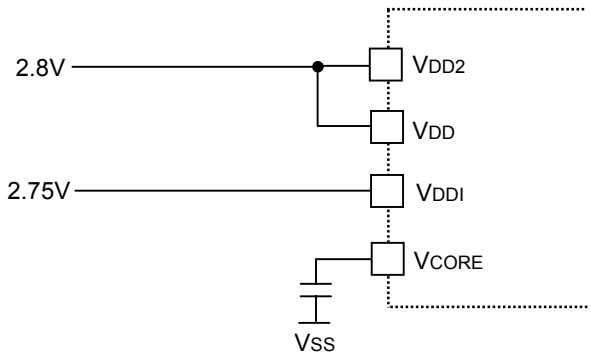
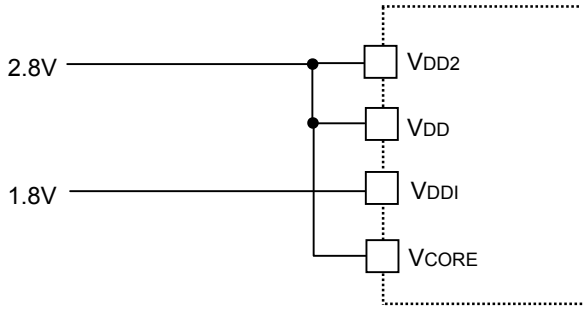


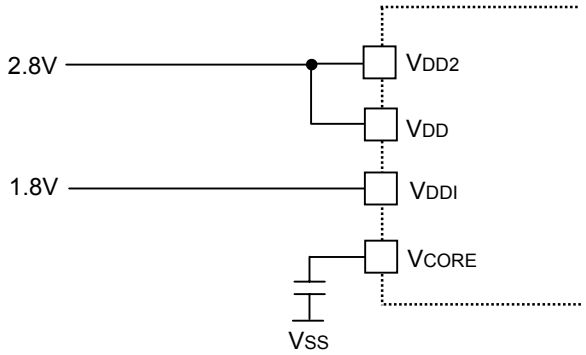
Fig.32 How to Connect to the External Power Supply Case (1)

Case (2) Two power supplies (One power supply is 1.65 to 2.3V.)
(Example AV_{DD} = 2.8V, DV_{DD} = 1.8V)

TEST3=H TEST4=L (V_{CORE} is normally OFF) : This connection should be used basically.



TEST3=L TEST4=H (V_{CORE} is normally ON)



TEST3=L TEST4=L (V_{CORE} automatic stop, automatic start)

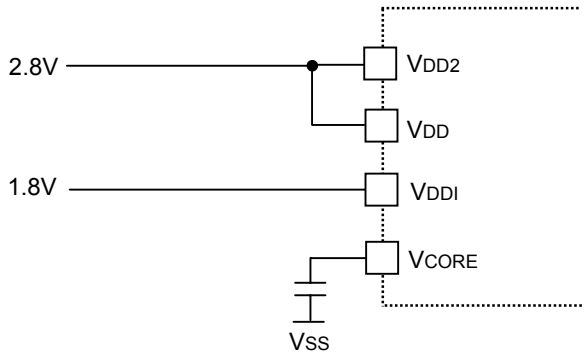
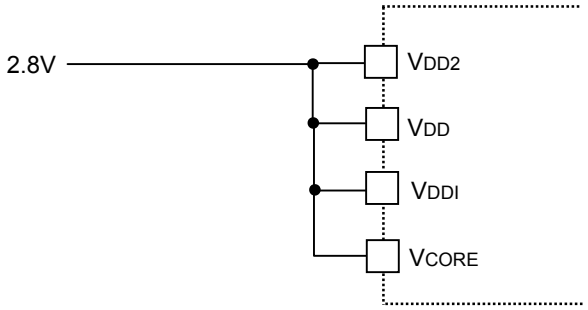


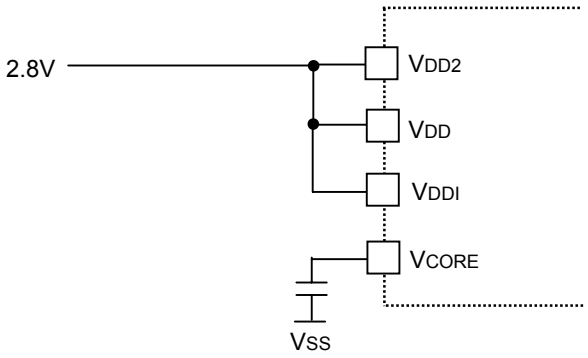
Fig.33 How to Connect to the External Power Supply Case (2)

Case (3) One power supply (2.3V or more is required)
(Example AV_{DD} = 2.8V)

TEST3=H TEST4=L (V_{CORE} is normally OFF) : This connection should be used basically.



TEST3=L TEST4=H (V_{CORE} is normally ON)



TEST3=L TEST4=L (V_{CORE} automatic stop, automatic start)

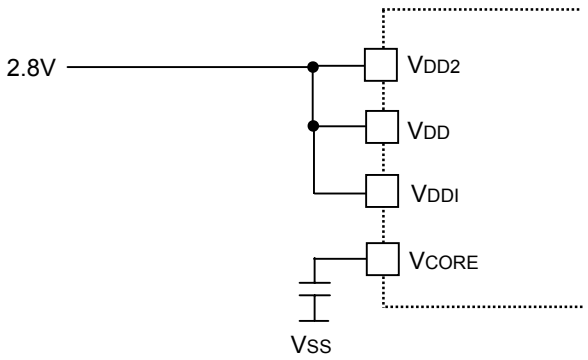


Fig.34 How to Connect to the External Power Supply Case (3)

6.8 Description of Operation of Built-in Power Supply

All bias voltages required for liquid crystal drive can be generated by single power input. The following voltage levels are generated.

Power supply for oscillation circuit: V_{OSC}
Reference power supply for 1st-boosting: V_{LDO} (It is not used and V_{DD2} is used usually)
Reference voltage: V_{REG}
Power supply: V_{OUT}, V_{OUTM}
Source driver voltage: V_{DDHS}, V_{DDRH}, V_{DDRL} and V_0 to V_{63}
Gate driver voltage: V_{DDHG}, V_{EE}, V_{ONREG} and V_{OFREG}
Voltage for opposed electrode: V_{COMH} and V_{COML}

The built-in electronic control function allows adjustment of each output voltage. The electronic control can be controlled by commands. The built-in reference voltage circuit permits continuously stable LCD power supply without depending on the system power supply. Built-in 1st, 2nd, 3rd, and 4th boosters provide high-precision constant voltage.

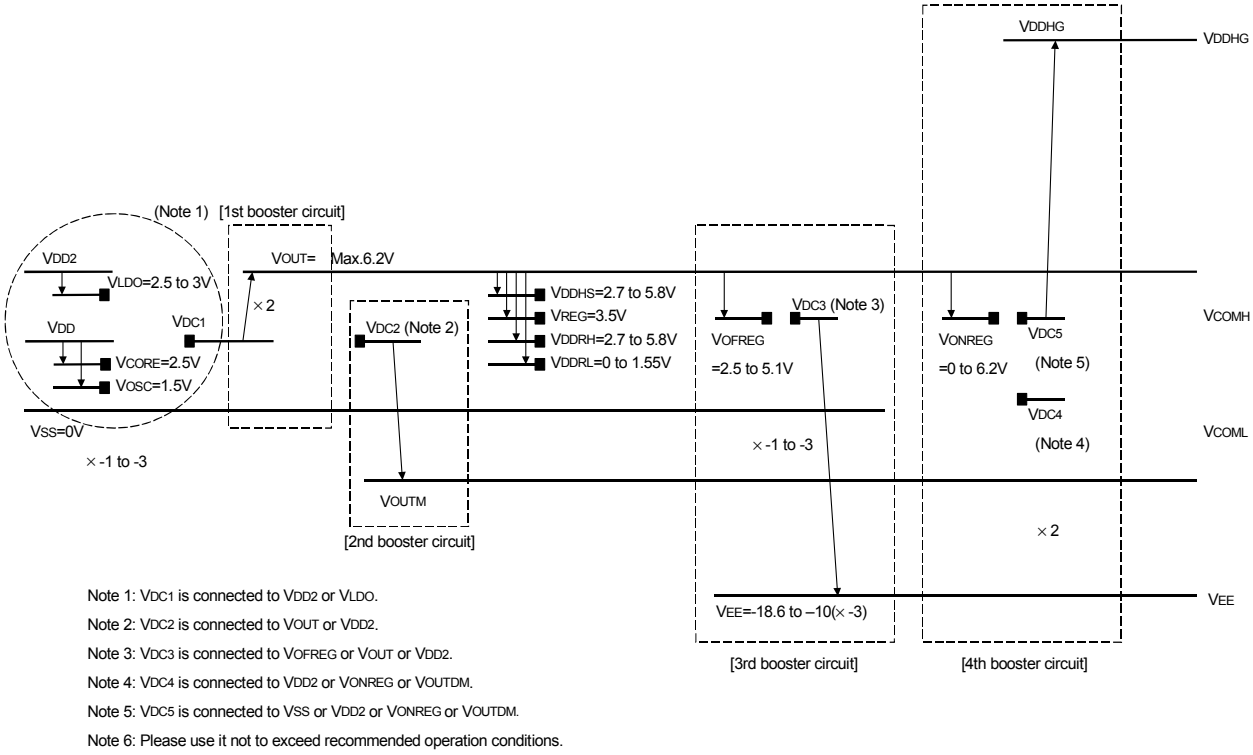


Fig.35 Voltage Relational Diagram

6.9 Power Supply for LCD and Main Specifications for Power Supply

Table 27 S1D19105 Power Supply for LCD and Main Specifications for Power Supply

No.	Parameter		S1D19105
1	Number of source lines for TFT panel		528 (176 RGB)
2	Number of gate lines for TFT panel		220
3	Structure of TFT panel holding capacity		Cst structure
4	LCD output	S1-S528	V_0 to V_{63} (analog 64 gray scale)
		G1-G220	Gate ON voltage: V_{DDHG} Gate OFF voltage: V_{EE}
		V_{COM}	Common HIGH voltage V_{COMH} Adjustment with the electronic control or external R Common LOW voltage V_{COML} Automatic setting with V_{COMH} - VCA × 2 Common amplitude: VCA × 2 Adjustment with electronic control
5	Input power supply	V_{DDI}	IO power supply
		V_{DD}	Power supply for V_{CORE} generation
		V_{DD2}	Reference power supply for booster circuit
6	Internal power supply output	V_{LDO}	Reference power supply for 1st boosting
		V_{CORE}	RAM and logic power supply.
		V_{OSC}	Power supply for oscillation
		V_{OUT} (1st booster output)	Power supply for source and V_{COM} generation V_{DD2} × double:
		V_{REG}	Reference voltage
		V_{DDHS}	Source driver power supply
		V_{DDRH}	Maximum gray scale voltage
		V_{DDRL}	Minimum gray scale voltage
		V_{COMH}	V_{COM} signal HIGH power supply
		V_{OFREG}	Reference voltage for V_{EE} generation
		V_{ONREG}	Reference voltage for V_{DDHG} generation
		V_{OUTM} (2nd booster output)	Power supply for V_{COML} generation -1 time boosting
		V_{COML}	V_{COM} signal LOW power supply
		V_{EE} (3rd booster output)	Gate OFF voltage -1 to 3 times boosting
		V_{DDHG} (4th booster output)	Gate ON voltage Double boosting

6.9.1 Basic Configuration Diagram of Built-in Power Supply

The S1D19105 contains a power supply circuit for liquid crystal drive. Select the external circuit configuration appropriate for your specifications by referring to the recommended basic circuits provided for stable use of built-in power circuit.

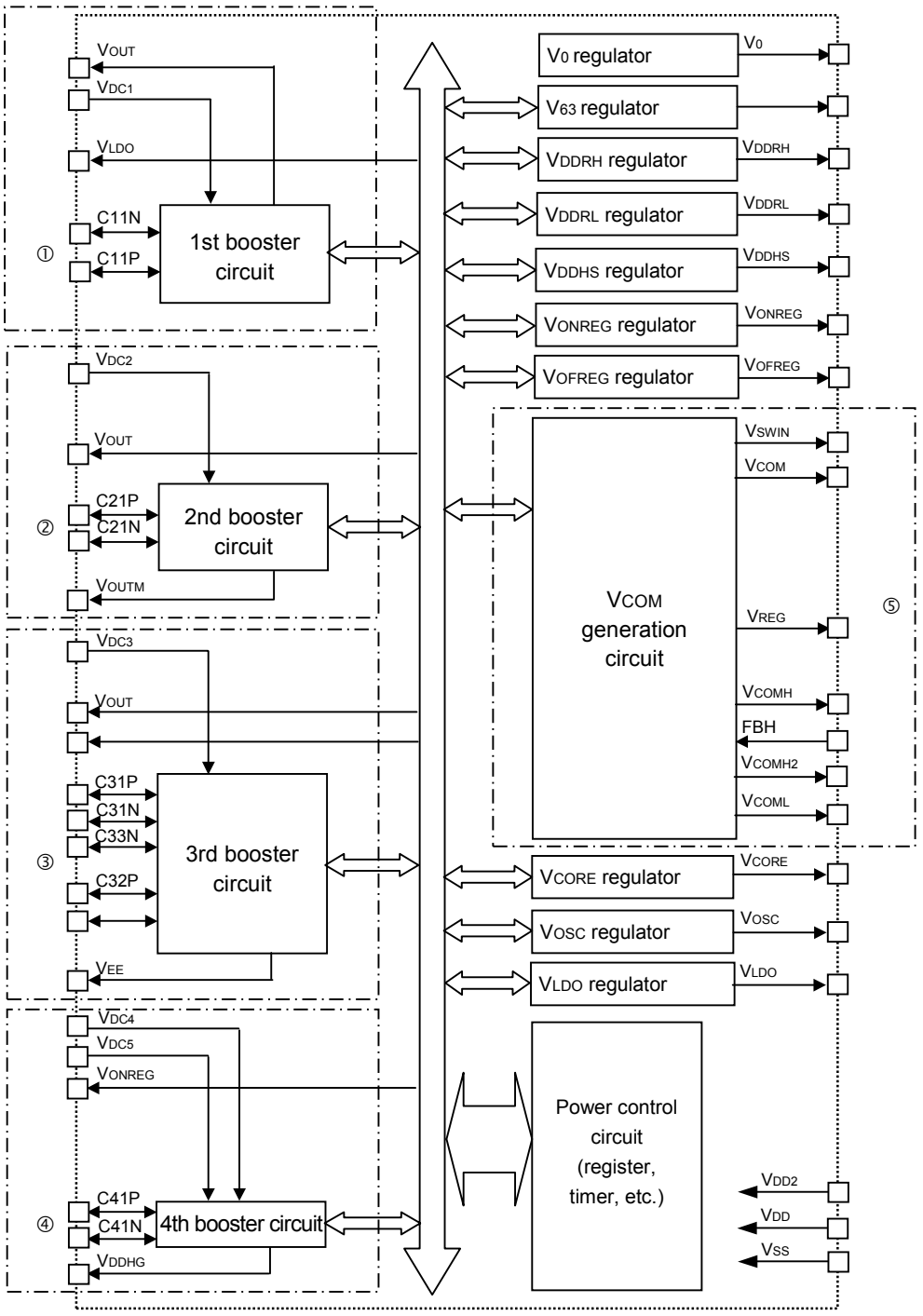


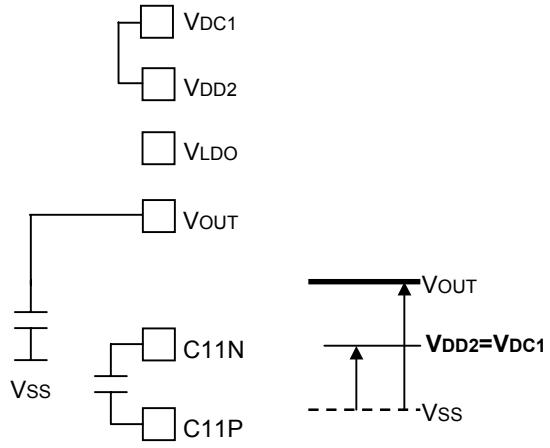
Fig. 36 Basic Configuration Diagram of Built-in Power Circuits

6.9.2 The 1st Booster Circuit

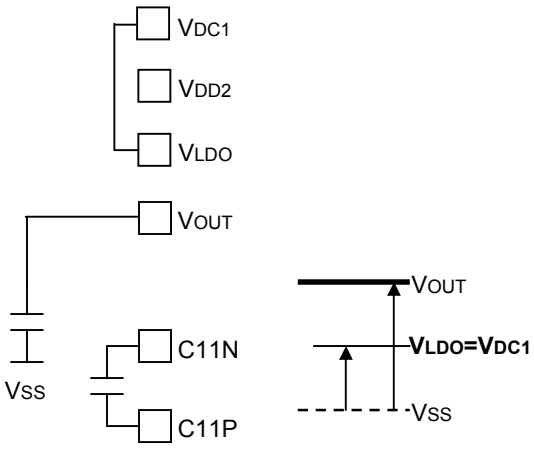
The 1st booster circuit, comprised of a charge pump type DC/DC converter, can be selected by external connection switching of the boost reference power supply. The booster converts the selected input power voltage (V_{DC1}) to the power supply for the liquid crystal power circuit (V_{OUT}) by doubling the voltage.

$$V_{OUT} = 2 \times V_{DC1} \text{ [V]}$$

The desired booster circuit is provided by changing the connection corresponding to ① in the basic configuration diagram of the internal power circuit.



Double boosting (V_{DC1} = V_{DD2})



Double boosting (V_{DC1} = V_{LDO})

Fig.37 The 1st Booster Circuit (Connection Example)

[V_{DC1} Select Voltage]
V_{DC1} should be selected V_{DD2} usually.

6.9.3 The 2nd Booster Circuit

The 2nd booster circuit, comprised of a charge pump type DC/DC converter, is a reverse booster circuit that can be selected by external connection switching of the boost reference power supply. The booster converts the selected input power voltage (between V_{DC2} and V_{SS}) to the power voltage (V_{OUTM}) for the V_{COM} circuit by multiplying the voltage by -1 time with reference to V_{SS}.

$$V_{OUTM} = -1 \times V_{DC2} \text{ [V]}$$

The desired circuit is provided by changing the connection corresponding to ② in the basic configuration diagram of the internal power circuit as shown below.

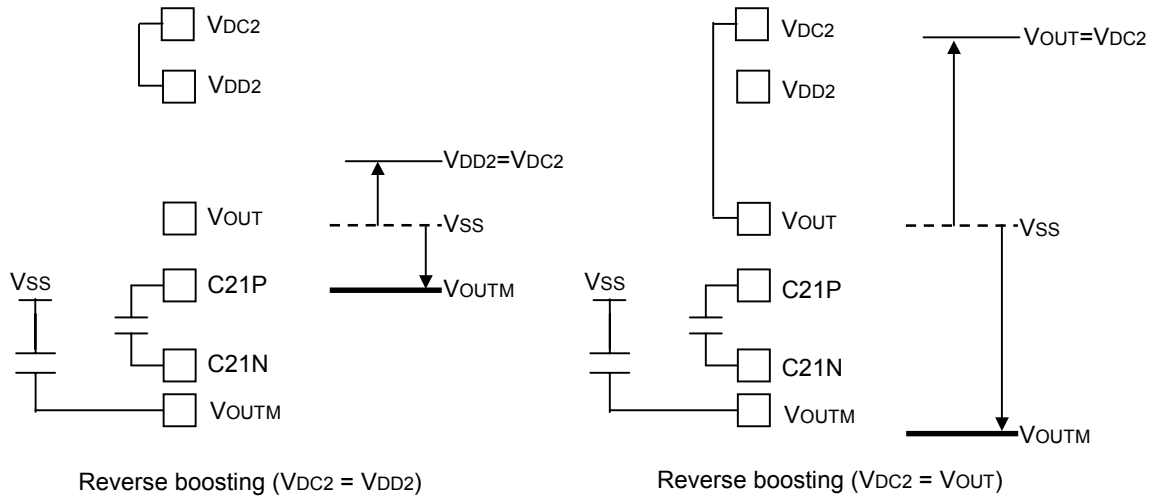


Fig.38 The 2nd Booster Circuit (Connection Example)

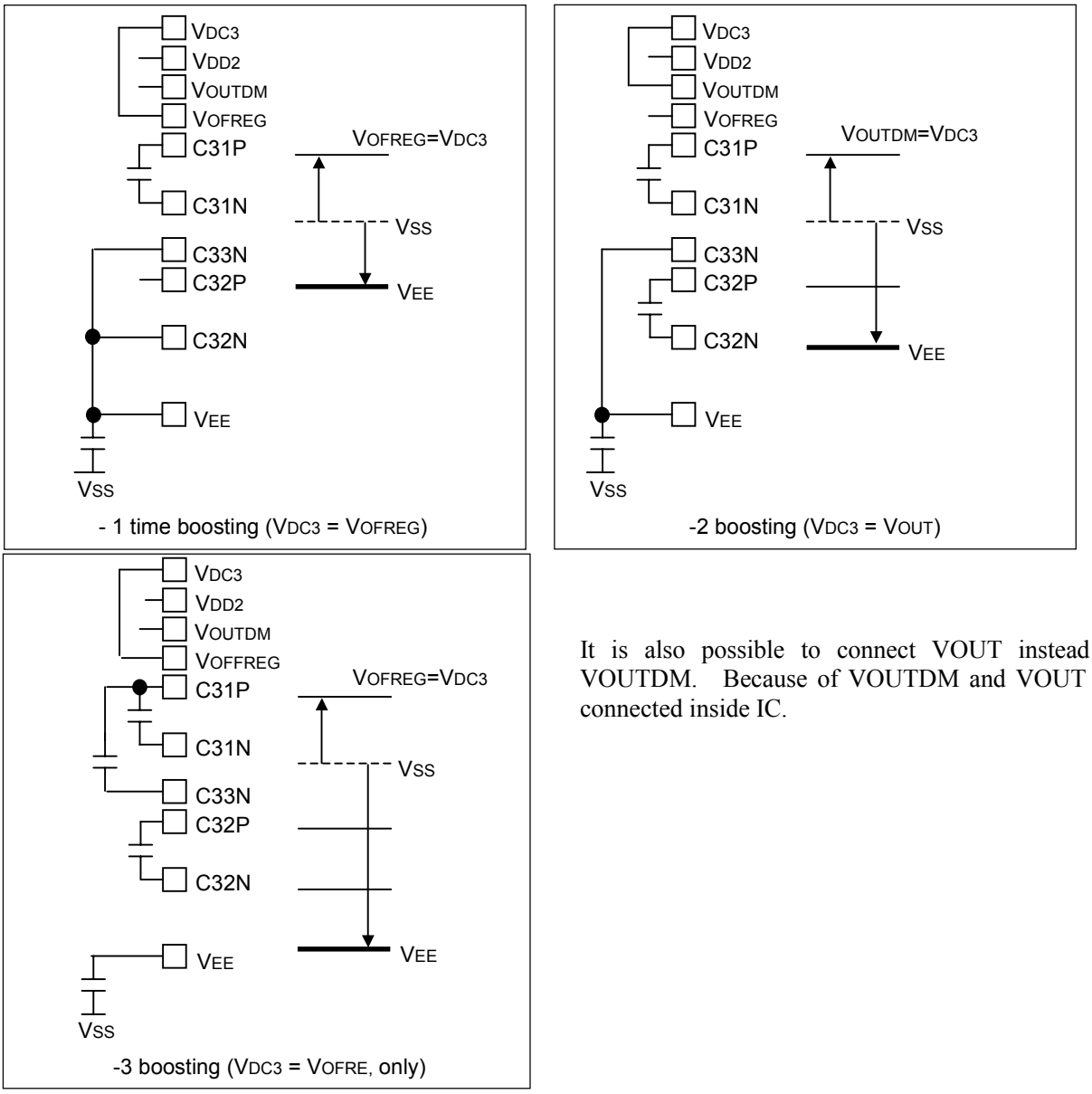
[V_{DC2} Select Voltage]
For V_{DC2}, V_{DD2} or V_{OUT} can be freely selected.

6.9.4 The 3rd Booster Circuit

The 3rd booster circuit, comprised of a charge pump type DC/DC converter, can be selected by external connection switching of the boost reference power supply. The booster converts the selected input power voltage (between V_{DC3} and V_{SS}) to the gate driver negative power voltage (V_{EE}) by -N times. Boosting by the magnifying power of -1, -2 and -3 is available through external connection.

$$V_{EE} = N \times V_{DC3} \text{ [V]} : [N = -1, -2, -3]$$

The desired circuit is provided by changing the connection corresponding to ③ in the basic configuration diagram of the internal power circuit as shown below.



It is also possible to connect VOUT instead of VOUTDM. Because of VOUTDM and VOUT are connected inside IC.

Fig.39 The 3rd Booster Circuit (Connection Example)

[V_{DC3} Select Voltage]
For V_{DC3}, select V_{DD2}, V_{OUTDM} and V_{OFREG} so that V_{DDHG} - $V_{EE} \leq 30.0V$ can be satisfied in any magnifying power of boosting. –3 times boosting should be set $V_{DC3} = V_{OFRE}$. Setting to $V_{OFREG} = V_{DC3}$ allows fine adjustment of the V_{EE} output voltage using the built-in regulator. The variable range of voltage is as follows.

V_{OFREG} output pin	2.0 to 5.1[V] (0.1 V step)	Built-in regulator output

6.9.5 The 4th Booster Circuit

The 4th booster circuit, comprised of a charge pump type DC/DC converter, is a reverse booster circuit that can be selected by external connection switching of the boost reference power supply. The booster converts the selected input power voltage (between V_{DC4} and V_{EE}) to the gate driver positive power voltage (V_{DDHG}) by 1 time with reference to V_{DC5}.

$$V_{DDHG} = V_{DC5} + 1 \times (V_{DC4}\text{-}V_{EE}) \text{ [V]}$$

The desired circuit is provided by changing the connection corresponding to ④ in the basic configuration diagram of the internal power circuit as shown below.

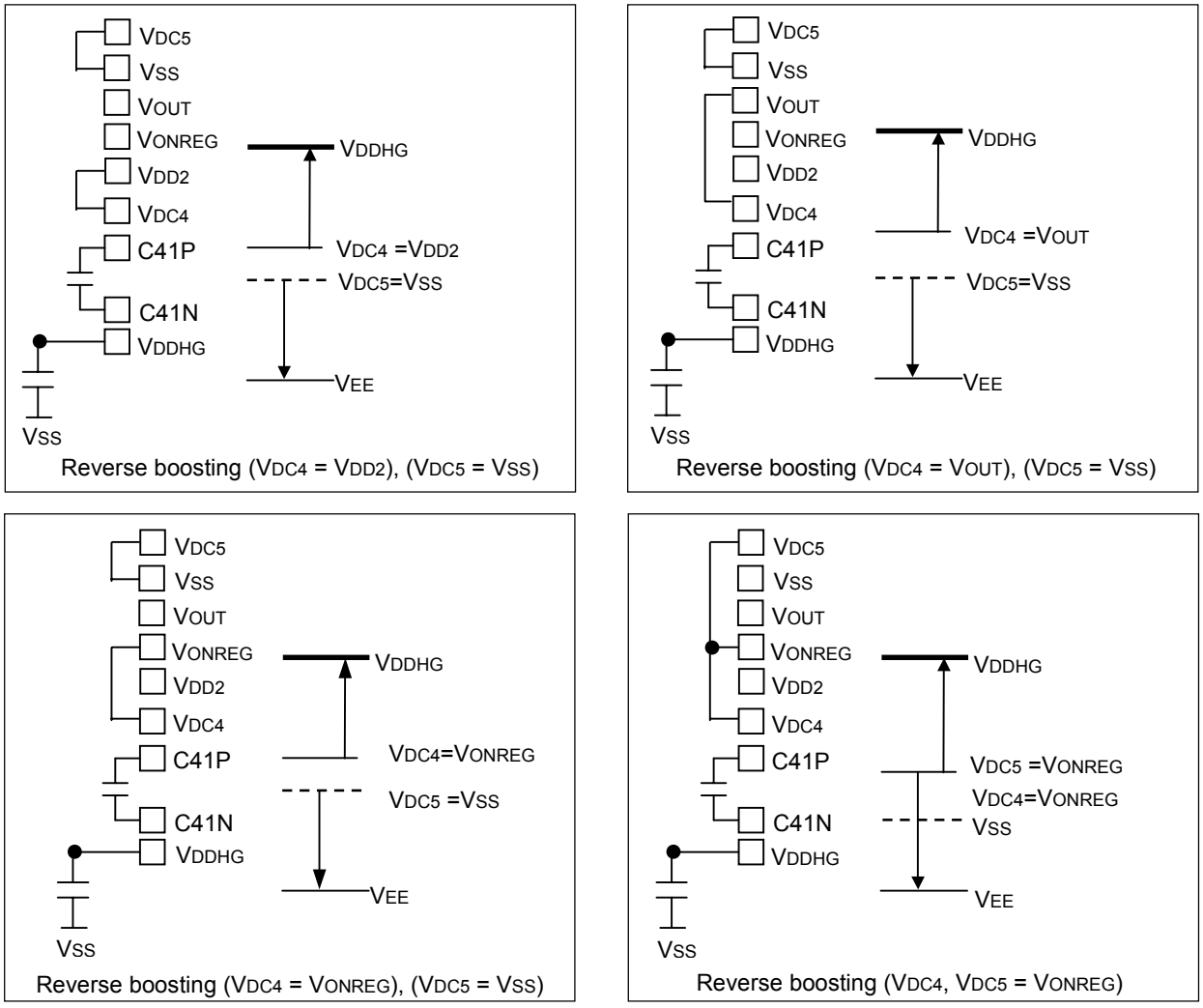


Fig.40 The 4th Booster Circuit (Connection Example)

[V_{DC4} Select Voltage]
For V_{DC4}, V_{DD2}, V_{SS} ,V_{ONREG} and V_{OUT} can be freely selected. In doing so, select the voltage to satisfy V_{DDHG} - V_{EE} ≤ 30.0V. Using V_{ONREG} allows fine adjustment of the V_{DDHG} voltage using the built-in regulator. VDC4 pin should connect more than 2.3V. When VDC4 pin needs to be used less than 2.3V, please connect with VONREG, set up VONREG more than 2.3V only at the time of boosting starting, and put in the processing adjusted to the target voltage by the electronic volume command or the power control command after the 4th boosting starting.

[V_{DC5} Select Voltage]
For V_{DC5}, V_{DD2}, V_{SS} ,V_{ONREG} and V_{OUT} can be freely selected. In doing so, select the voltage to satisfy V_{DDHG} - V_{EE} ≤ 30.0V. Using V_{ONREG} allows fine adjustment of the V_{DDHG} voltage using the built-in regulator. The variable range of the voltage is as follows.

V_{ONREG} output pin	0.0 to 6.2[V] (0.2 V step)	Built-in regulator output

6.9.6 VCOM Generation Circuit

The VCOM generation circuit generates the voltage of VCOMH and VCOML needed for generating VCOM output voltage. Setting of each voltage can be combined as follows.

VCOMH: Electronic control register setting using the built-in resistor
Adjustment of output voltage through external resistor
VCOML: VCOML = VCOMH - VCA × 2 [V]

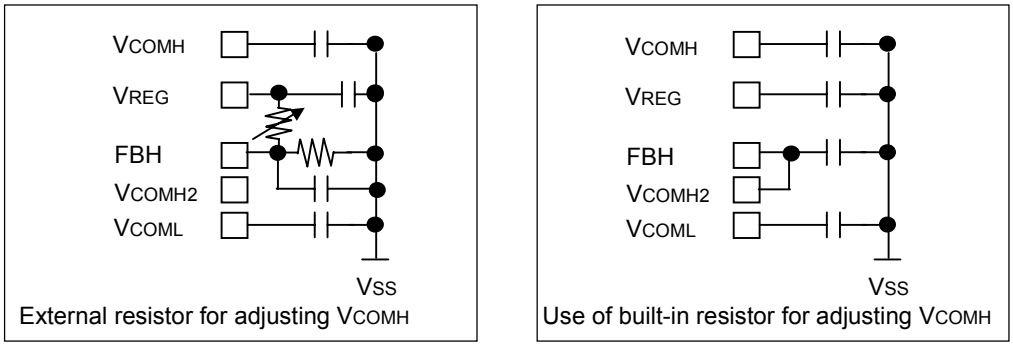


Fig.41 VCOM Generation Circuit (Connection Example)

VCOMH output pin	2.0 to 5.975[V] (0.075 V step)	Built-in regulator output

6.10 Connection Diagram of External Parts

External Circuit Connection Example 1

Specifications: 1st booster circuit [V_{DC1} select = V_{DD2}]
2nd booster circuit [V_{DC2} select = V_{DD2}]
3rd booster circuit [V_{DC3} select = V_{OUT}, -double boosting mode]
4th booster circuit [V_{DC4} select = V_{DD2}, V_{DC5} select = V_{SS}]
V_{COM} generation circuit [Specifications for external resistor for adjusting V_{COMH}]

Example) Assuming that V_{DD2} = 2,85V, each voltage with no load is as follows.

V_{OUT}	$= 2 \times V_{DD2}$	=	5.7[V]
V_{OUTM}	$= -1 \times V_{DD2}$	=	-2.85[V]
V_{EE}	$= -2 \times V_{OUT}$	=	-11.4[V]
V_{DDHG}	$= V_{DC5} + 1 \times (V_{DC4} - V_{EE})$	=	14.25[V]

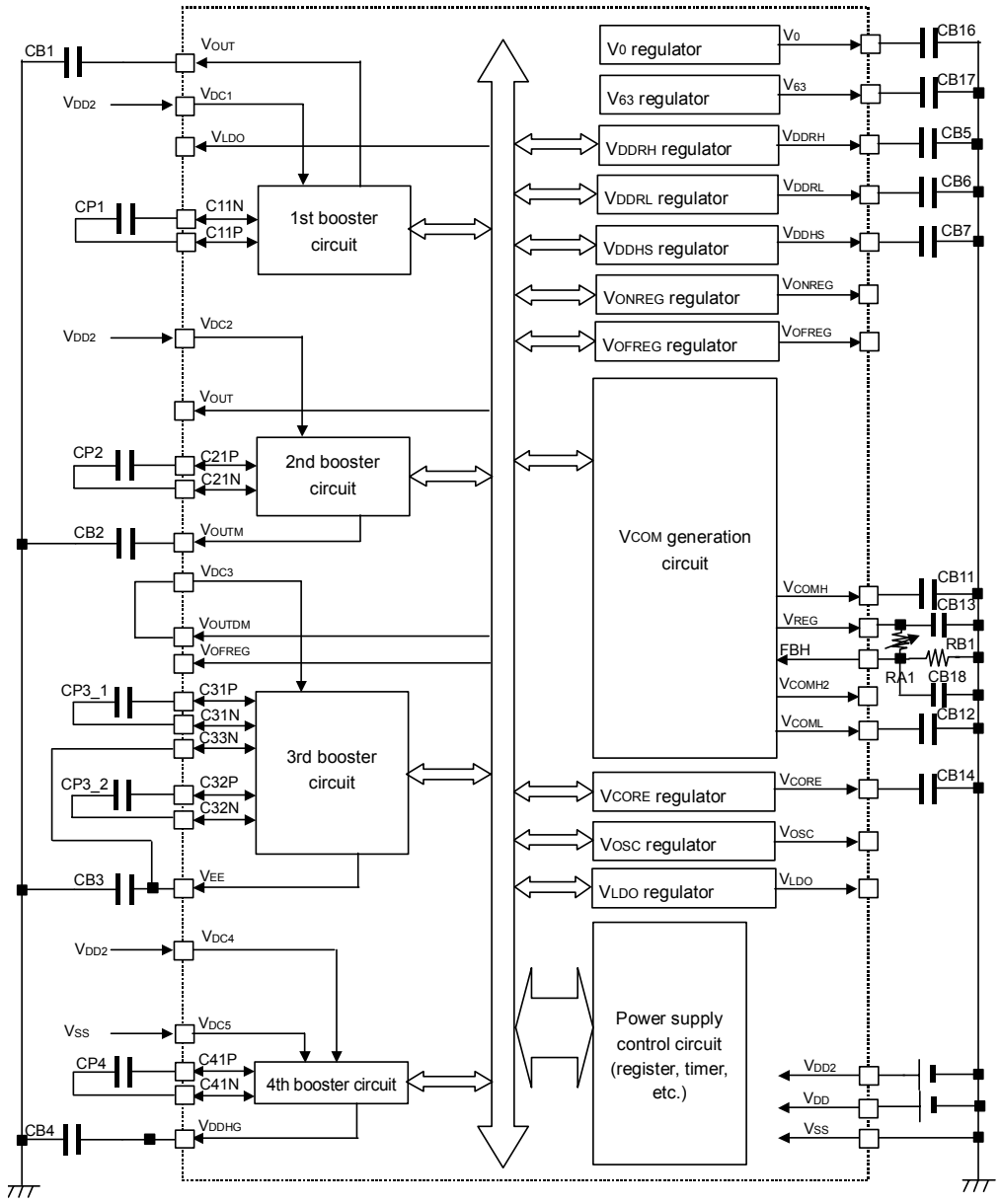


Fig.42 External Circuit Connection Example 1

External Circuit Connection Example 2

Specifications: 1st booster circuit [V_{DC1} select = V_{LDO}]
2nd booster circuit [V_{DC2} select = V_{OUT}]
3rd booster circuit [V_{DC3} select = V_{OFREG}, -triple boosting mode]
4th booster circuit [V_{DC4} select = V_{ONREG}, V_{DC5} select = V_{SS}]
V_{COM} generation circuit [Specifications for built-in resistor for adjusting V_{COMH}]

Example) Assuming that V_{DD2} = 2.85V, each voltage with no load is as follows.

V_{LDO}	= 2.55V(Typ.)	[Regulator output]
V_{OFREG}	= 4.0V	[Regulator output (Electronic control setting)]
V_{ONREG}	= 3.0V	[Regulator output (Electronic control setting)]
V_{OUT}	= 2 × V_{LDO}	= 5.1[V]
V_{OUTM}	= -1 × V_{OUT}	= -5.1[V]
V_{EE}	= -3 × V_{OFREG}	= -12.0[V]
V_{DDHG}	= V_{ONREG} - V_{EE}	= 15.0[V]

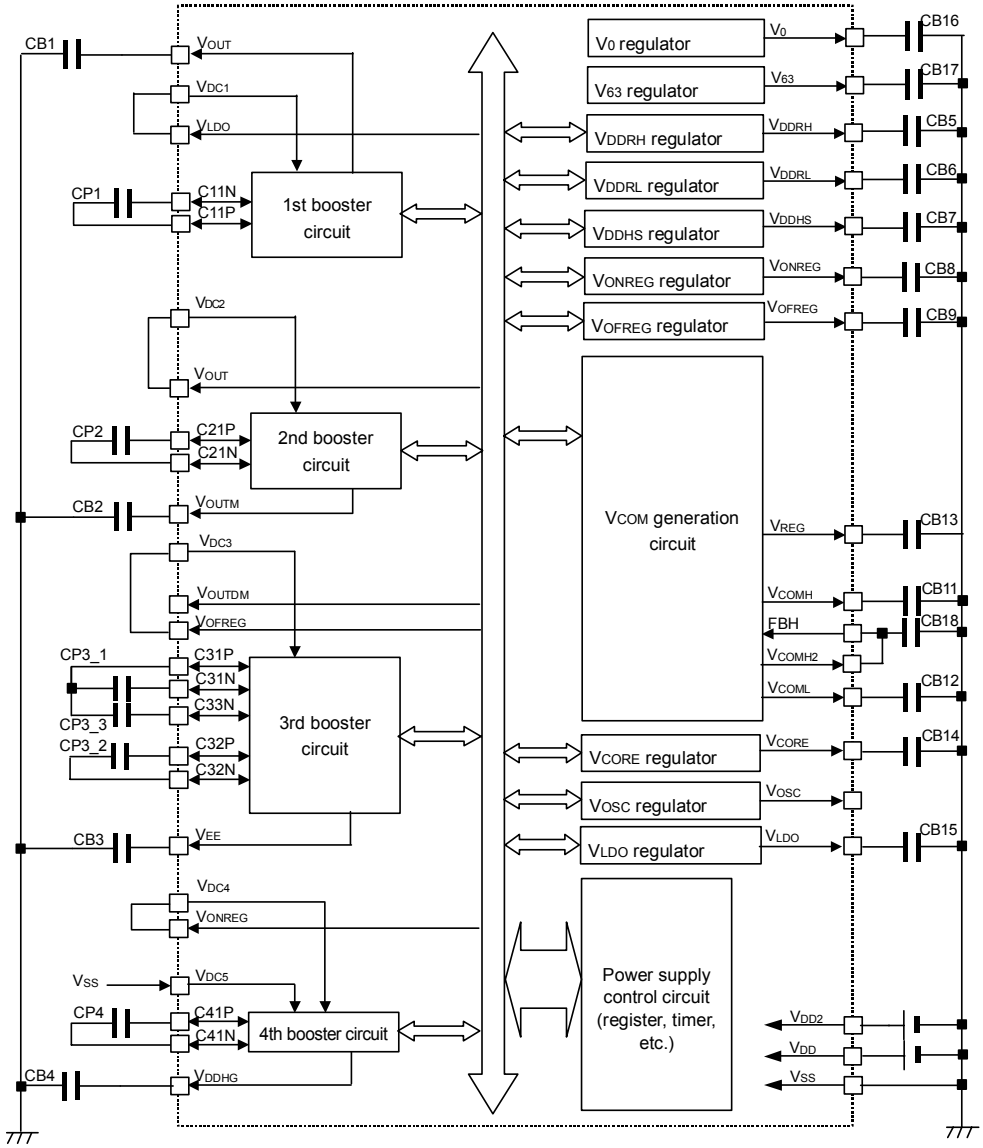


Fig.43 External Circuit Connection Example 2

Table 28 Recommended Capacity Value

Circuit name	Capacitor name	Capacity value [µF]	Maximum value of voltage biased to both ends of the capacitor
1st booster output	CP1	1.0 to 2.2	V_{DD2}, V_{LDO}
	CB1	1.0 to 2.2	V_{DD2}×2, V_{LDO}×2
2nd booster output	CP2	1.0 to 2.2	V_{DD2}, V_{OUT}
	CB2	1.0 to 2.2	V_{DD2}, V_{OUT}
3rd booster output	CP3_1	1.0	V_{DD2}, V_{OUT}, V_{OFREG}
	CP3_2	1.0	V_{DD2}×2, V_{OUT}×2, V_{OFREG}×2
	CP3_3	1.0	V_{OFREG}×3
	CB3	1.0	V_{DD2}×2, V_{OUT}×2, V_{OFREG}×3
4th booster output	CP4	0.1 to 1.0	V_{DC4} - V_{EE}
	CB4	0.1 to 1.0	V_{DC5} + (V_{DC4} - V_{EE})
V_{COM} generation circuit	CB18	0.01 to 0.1	FBH
	CB11	1.0 to 2.2	V_{COMH}
	CB12	1.0 to 2.2	V_{COML}
	CB13	0.1 to 1.0	V_{REG}
Regulator	CB5	1.0	V_{DDRH}
	CB6	0.1	V_{DDRL}
	CB7	1.0 to 2.2	V_{DDHS}
	CB8	0.1 to 1.0	V_{ONREG}
	CB9	0.1 to 1.0	V_{OFREG}
Power supply	CB14	1.0 to 2.2	V_{CORE}
	CB15	1.0 to 2.2	V_{LDO}
Gray scale	CB16	0.1	V_0
	CB17	0.1	V_{63}

The maximum voltage can be set when using the built-in electronic control if V_{REG} = 3.5V. V_{REG} does not include variations.
The capacity of the capacitor is the recommended value. When selecting a capacitor, check the appearance quality of indication with the actual equipment and set to the capacity value that makes the voltage of liquid crystal drive stable.
Use the B characteristics for capacitor.
A tolerance voltage should be selected aiming at 70% of the standard.

Table 30 Recommended Value for Wiring Resistor when Installing COG

Pin type	Pin name, etc.	Pin number	Resistor value
Power pins	V_{DDI}	40, 41, 136 to 139	10Ω or less
	V_{SS}	42 to 45, 128 to 135	
	V_{CORE}	36 to 39, 140 to 147	
	V_{DD}, V_{DD2}	148 to 163	
Booster series pins	1st booster pins	164 to 179	10Ω or less
	2nd booster pins	182 to 189	20Ω or less
	3rd and 4th booster pins	7 to 35(Except DUMMY)	30Ω or less
	V_{COM} auxiliary pins, etc.	198 to 200	20Ω or less
Other logic signal pins	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$	Others	100Ω or less
	D0 to D17,V_{DD},V_{SS}, etc.		

The above values are recommended, however, it does not mean that the resistor does not function if they are not satisfied.
Since the booster-series pins are effective for power conversion efficiency, the lower the value is, the better the efficiency becomes.
Since impedance is high in wiring to the FBH pin, carry out wiring as short as possible to prevent the influence of noise.
Also, prevent wiring from crossing other signals.

6.11 Gray scale Voltage Generation Circuit

This circuit generates 64 levels by 2 series (positive and negative poles) of voltages according to the polarity inversion for AC operation. The circuit incorporates a function to correct the gray scale voltage curve according to the characteristics of panel to be connected. Setting can be changed using the Set Gamma Correction Characteristics command. However, care should be taken, because power consumption is so high that can cause departure from the default γ ratio. The reference voltage circuit (positive pole) configuration diagram is shown below. Negative pole also serves as an equivalent composition figure.

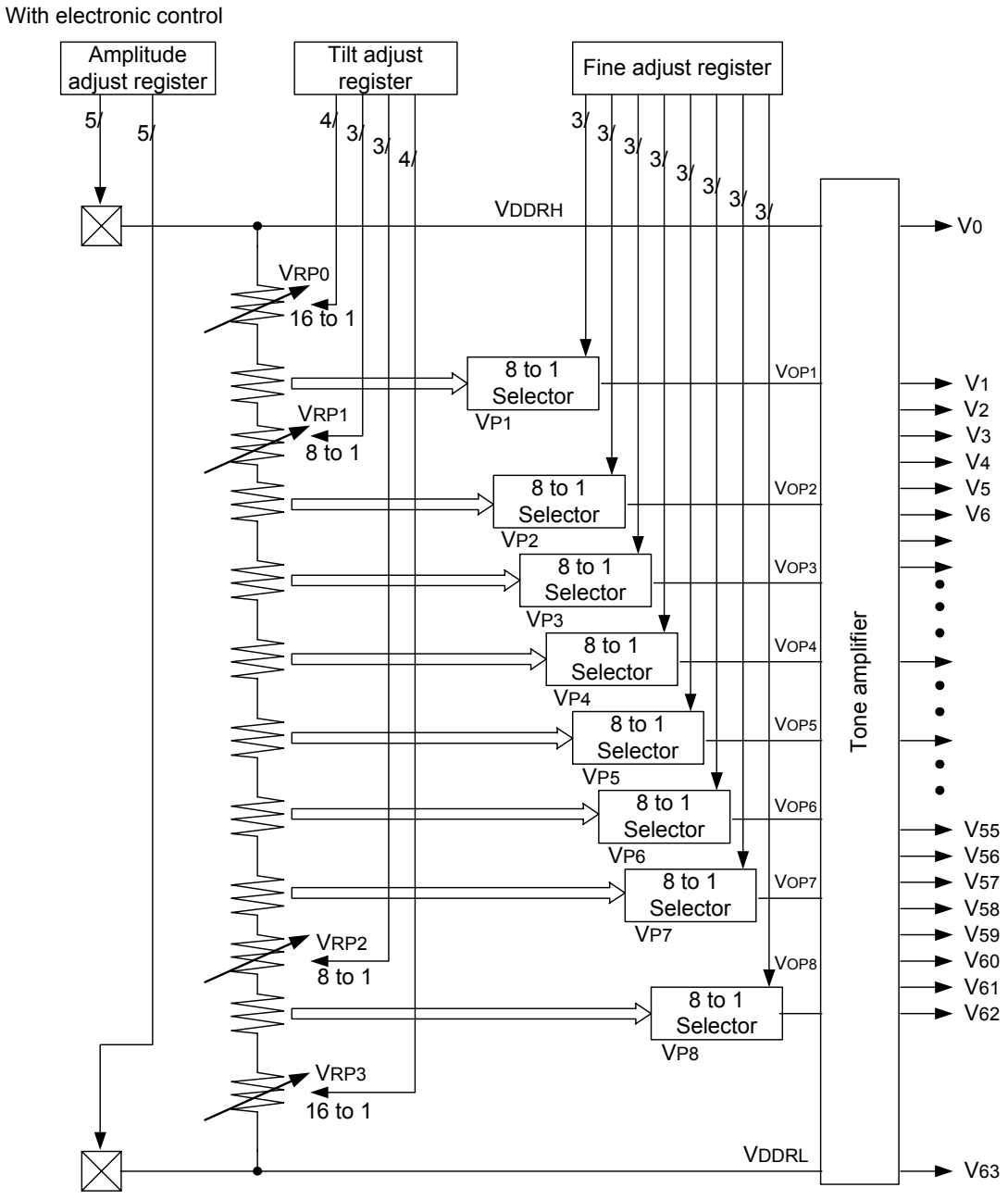


Fig.44 Reference Voltage Circuit Configuration Diagram (Positive Pole)

6.11.1 Adjusting Gray Scale Voltage

Adjustment of gray scale voltage and tilt as well as fine adjustment are available in accordance with characteristics of liquid crystal panel or color creation.

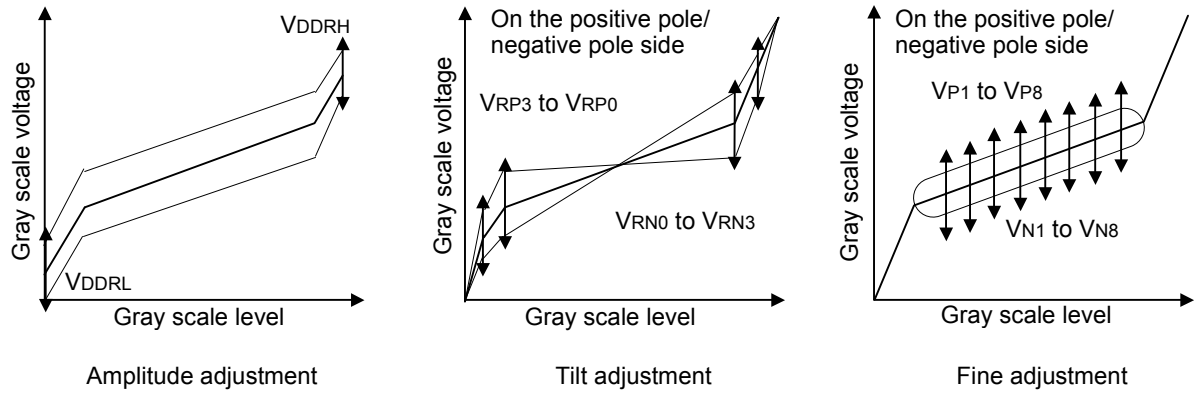


Fig.45 Gray scale Voltage Slope Adjustment

6.11.2 Amplitude Adjustment

Determines with the electronic control command.

6.11.3 Tilt Adjustment

Adjusts the tilt of the gray scale voltage for four points of the gray scale level.

6.11.4 Fine Adjustment of Gray Scale Voltage

Fine-adjusts the gray scale voltage for eight points of the gray scale level. At each point, fine adjustment is made by selecting one of 8 types (4 or 3 bits) of the voltage generated by the resistance string.

6.12 Calculation of Gray Scale Voltage

Specifying the gray scale voltage involves three registers. The amplitude register determines the entire difference of voltage, the tilt adjust register determines a tilt of gray scale curve by selecting internal fixed resistor, and the voltage fine-adjust register for fine adjusting the gray scale voltage.

■ Amplitude Adjustment

The Set Electronic Control commands allows adjustment of amplitude of V_{DDRH} and V_{DDRL} (5 bits: Specify a value of 0 to 31). Therefore, the value to be changed is within V_{DDRH} - V_{DDRL}.

V_{DDRH} : 2.70V to 5.80V

V_{DDRL} : 0.00V to 1.55V

■ Tilt Adjust Register

Specify the resistor value using V_{RP0} (4 bits), V_{RP1} (3 bits), V_{RP2} (3 bits) and V_{RP3} (4 bits).

Table 30 Tilt Adjust Register Value and Resistor Value (Colored items indicate the standard value.)

Tilt adjust register		Resistor value
V_{RP0}<3:0>	0000	1R
	0001	3R
	0010	5R
	0011	7R
	0100	9R
	0101	12R
	0110	16R
	0111	21R
	1000	27R
	1001	34R
	1010	42R
	1011	52R
	1100	64R
	1101	78R
	1110	96R
	1111	120R
V_{RP1}<2:0>	000	0R
	001	4R
	010	8R
	011	12R
	100	16R
	101	20R
	110	25R
	111	30R

Tilt adjust register		Resistor value
V_{RP2}<2:0>	000	0R
	001	4R
	010	8R
	011	12R
	100	16R
	101	20R
	110	25R
	111	30R
V_{RP3}<3:0>	0000	1R
	0001	3R
	0010	5R
	0011	7R
	0100	9R
	0101	12R
	0110	16R
	0111	21R
	1000	27R
	1001	34R
	1010	42R
	1011	52R
	1100	64R
	1101	78R
	1110	96R
	1111	120R

■ Voltage Fine-Adjust Register

Select the reference voltage V_{OP1} to V_{OP8} to the gray scale amplifier with the fine-adjust register (3 bits). The expression for calculation is shown below. SUMRP of the expression means the value of four variable resistors for tilt adjustment with the basic R added.

Tilt adjust resistor	Min.	Max.	Typ.
V_{RP0}	1R	120R	5R
V_{RP1}	0R	30R	0R
V_{RP2}	0R	30R	0R
V_{RP3}	1R	120R	7R
Basic R	—	—	126R

$SUMRP = V_{RP0} + V_{RP1} + V_{RP2} + V_{RP3} + Basic\ R$

	Fine-adjust register		Expression for calculation
V_{DDRH}			V_{DDRH}
V_{OP1}	V_{P1}<2:0>	000	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+0R)/SUMRP$
		001	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+2R)/SUMRP$
		010	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+4R)/SUMRP$
		011	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+6R)/SUMRP$
		100	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+8R)/SUMRP$
		101	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+10R)/SUMRP$
		110	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+12R)/SUMRP$
		111	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+14R)/SUMRP$
V_{OP2}	V_{P2}<2:0>	000	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+16R+V_{RP1})/SUMRP$
		001	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+18R+V_{RP1})/SUMRP$
		010	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+20R+V_{RP1})/SUMRP$
		011	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+22R+V_{RP1})/SUMRP$
		100	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+24R+V_{RP1})/SUMRP$
		101	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+26R+V_{RP1})/SUMRP$
		110	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+28R+V_{RP1})/SUMRP$
		111	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+30R+V_{RP1})/SUMRP$
V_{OP3}	V_{P3}<2:0>	000	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+32R+V_{RP1})/SUMRP$
		001	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+34R+V_{RP1})/SUMRP$
		010	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+36R+V_{RP1})/SUMRP$
		011	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+38R+V_{RP1})/SUMRP$
		100	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+40R+V_{RP1})/SUMRP$
		101	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+42R+V_{RP1})/SUMRP$
		110	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+44R+V_{RP1})/SUMRP$
		111	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+46R+V_{RP1})/SUMRP$
V_{OP4}	V_{P4}<2:0>	000	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+48R+V_{RP1})/SUMRP$
		001	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+50R+V_{RP1})/SUMRP$
		010	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+52R+V_{RP1})/SUMRP$
		011	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+54R+V_{RP1})/SUMRP$
		100	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+56R+V_{RP1})/SUMRP$
		101	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+58R+V_{RP1})/SUMRP$
		110	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+60R+V_{RP1})/SUMRP$
		111	$V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+62R+V_{RP1})/SUMRP$

	Fine-adjust register		Expression for calculation
V_{OP5}	V_{P5}<2:0>	000	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+64R+V_{RP1})/SUMRP
		001	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+66R+V_{RP1})/SUMRP
		010	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+68R+V_{RP1})/SUMRP
		011	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+70R+V_{RP1})/SUMRP
		100	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+72R+V_{RP1})/SUMRP
		101	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+74R+V_{RP1})/SUMRP
		110	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+76R+V_{RP1})/SUMRP
		111	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+78R+V_{RP1})/SUMRP
V_{OP6}	V_{P6}<2:0>	000	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+80R+V_{RP1})/SUMRP
		001	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+82R+V_{RP1})/SUMRP
		010	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+84R+V_{RP1})/SUMRP
		011	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+86R+V_{RP1})/SUMRP
		100	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+88R+V_{RP1})/SUMRP
		101	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+90R+V_{RP1})/SUMRP
		110	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+92R+V_{RP1})/SUMRP
		111	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+94R+V_{RP1})/SUMRP
V_{OP7}	V_{P7}<2:0>	000	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+96R+V_{RP1})/SUMRP
		001	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+98R+V_{RP1})/SUMRP
		010	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+100R+V_{RP1})/SUMRP
		011	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+102R+V_{RP1})/SUMRP
		100	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+104R+V_{RP1})/SUMRP
		101	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+106R+V_{RP1})/SUMRP
		110	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+108R+V_{RP1})/SUMRP
		111	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+110R+V_{RP1})/SUMRP
V_{OP8}	V_{P8}<2:0>	000	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+112R+V_{RP1}+V_{RP2})/SUMRP
		001	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+114R+V_{RP1}+V_{RP2})/SUMRP
		010	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+116R+V_{RP1}+V_{RP2})/SUMRP
		011	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+118R+V_{RP1}+V_{RP2})/SUMRP
		100	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+120R+V_{RP1}+V_{RP2})/SUMRP
		101	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+122R+V_{RP1}+V_{RP2})/SUMRP
		110	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+124R+V_{RP1}+V_{RP2})/SUMRP
		111	V_{DDRH}-(V_{DDRH}-V_{DDRL}) * (V_{RP0}+126R+V_{RP1}+V_{RP2})/SUMRP
V_{DDRL}			V_{DDRL}

■ Gray Scale Voltage

The expression for calculating the gray scale voltage is shown below.

Gray scale voltage	Expression for calculation
V_0	V_{DDRH}
V_1	V_{OP1}
V_2	$V_{OP2}+(V_{OP1}-V_{OP2}) * (27/38)$
V_3	$V_{OP2}+(V_{OP1}-V_{OP2}) * (19/38)$
V_4	$V_{OP2}+(V_{OP1}-V_{OP2}) * (12/38)$
V_5	$V_{OP2}+(V_{OP1}-V_{OP2}) * (5/38)$
	V_{OP2}
V_6	$V_{OP3}+(V_{OP2}-V_{OP3}) * (37/38)$
V_7	$V_{OP3}+(V_{OP2}-V_{OP3}) * (31/38)$
V_8	$V_{OP3}+(V_{OP2}-V_{OP3}) * (24/38)$
V_9	$V_{OP3}+(V_{OP2}-V_{OP3}) * (19/38)$
V_{10}	$V_{OP3}+(V_{OP2}-V_{OP3}) * (13/38)$
V_{11}	$V_{OP3}+(V_{OP2}-V_{OP3}) * (8/38)$
V_{12}	$V_{OP3}+(V_{OP2}-V_{OP3}) * (3/38)$
	V_{OP3}
V_{13}	$V_{OP4}+(V_{OP3}-V_{OP4}) * (36/38)$
V_{14}	$V_{OP4}+(V_{OP3}-V_{OP4}) * (31/38)$
V_{15}	$V_{OP4}+(V_{OP3}-V_{OP4}) * (27/38)$
V_{16}	$V_{OP4}+(V_{OP3}-V_{OP4}) * (23/38)$
V_{17}	$V_{OP4}+(V_{OP3}-V_{OP4}) * (19/38)$
V_{18}	$V_{OP4}+(V_{OP3}-V_{OP4}) * (15/38)$
V_{19}	$V_{OP4}+(V_{OP3}-V_{OP4}) * (12/38)$
V_{20}	$V_{OP4}+(V_{OP3}-V_{OP4}) * (8/38)$
V_{21}	$V_{OP4}+(V_{OP3}-V_{OP4}) * (5/38)$
V_{22}	$V_{OP4}+(V_{OP3}-V_{OP4}) * (2/38)$
	V_{OP4}
V_{23}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (37/38)$
V_{24}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (34/38)$
V_{25}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (31/38)$
V_{26}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (28/38)$
V_{27}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (24/38)$
V_{28}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (21/38)$
V_{29}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (18/38)$
V_{30}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (16/38)$
V_{31}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (13/38)$
V_{32}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (10/38)$
V_{33}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (7/38)$
V_{34}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (4/38)$
V_{35}	$V_{OP5}+(V_{OP4}-V_{OP5}) * (1/38)$

Gray scale voltage	Expression for calculation
	V_{OP5}
V_{36}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (36/38)$
V_{37}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (33/38)$
V_{38}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (30/38)$
V_{39}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (27/38)$
V_{40}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (24/38)$
V_{41}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (22/38)$
V_{42}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (19/38)$
V_{43}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (16/38)$
V_{44}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (13/38)$
V_{45}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (10/38)$
V_{46}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (6/38)$
V_{47}	$V_{OP6}+(V_{OP5}-V_{OP6}) * (3/38)$
	V_{OP6}
V_{48}	$V_{OP7}+(V_{OP6}-V_{OP7}) * (38/38)$
V_{49}	$V_{OP7}+(V_{OP6}-V_{OP7}) * (34/38)$
V_{50}	$V_{OP7}+(V_{OP6}-V_{OP7}) * (31/38)$
V_{51}	$V_{OP7}+(V_{OP6}-V_{OP7}) * (27/38)$
V_{52}	$V_{OP7}+(V_{OP6}-V_{OP7}) * (23/38)$
V_{53}	$V_{OP7}+(V_{OP6}-V_{OP7}) * (20/38)$
V_{54}	$V_{OP7}+(V_{OP6}-V_{OP7}) * (16/38)$
V_{55}	$V_{OP7}+(V_{OP6}-V_{OP7}) * (12/38)$
V_{56}	$V_{OP7}+(V_{OP6}-V_{OP7}) * (7/38)$
V_{57}	$V_{OP7}+(V_{OP6}-V_{OP7}) * (2/38)$
	V_{OP7}
V_{58}	$V_{OP8}+(V_{OP7}-V_{OP8}) * (35/38)$
V_{59}	$V_{OP8}+(V_{OP7}-V_{OP8}) * (28/38)$
V_{60}	$V_{OP8}+(V_{OP7}-V_{OP8}) * (21/38)$
V_{61}	$V_{OP8}+(V_{OP7}-V_{OP8}) * (12/38)$
V_{62}	V_{OP8}
V_{63}	V_{DDRL}

The constant 38 in the expression for calculation indicates the total number of bits in the tilt register and fine-adjust register.

6.13 Resetting

When the power is turned on, resetting by the $\overline{RES}$ pin is necessary. Following the rest by the $\overline{RES}$ pin, each input pin must be normally controlled. For connection of the LOW pulse width for reset, continue 1µs or more. If it is 100ns or less, it is rejected.

For the default value of the command and parameter after reset, see
(1) 7.2 Initial Values of a Single-Byte Command
(2) 7.3 Parameter Initial Value List.

During reset ($\overline{RES}$ = LOW), no data is output even if revision read operation is performed. It becomes Hi-Z.

7. COMMANDS

The data bus signal is identified by combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) pins. All commands are interpreted and executed independent from external clocks. When A0 is LOW, data existing on the data bus is considered to be a command. When A0 is HIGH, data is considered to be a command parameter or the data of display data RAM.

Each of commands and parameters is defined in a single byte (8 bits) long. Pins D0 to D9 are invalid for 16-bit or 18-bit parallel interfacing. Eight bits after the D/C are valid for serial interfacing.

There are two types of commands: multiple-byte commands having parameters, and single-byte commands having no parameters. To issue a multiple-byte command, enter its single-byte command code and enter the specified number of bytes of parameters. If there are two or more parameters, all parameters must be entered, in principle. Another command can also be entered during parameter entry if A0 is set to LOW by accessing via $\overline{WR}$ or E signal. However, it should be noted that for parameters to be executed in synchronization with VSYNC, those parameters entered partway are not executed. The parameter to be executed in synchronization with VSYNC is executed in synchronization with the first VSYNC after all the parameters have been entered.

The RAM Write and RAM Read commands have not restriction in the number of parameter bytes. The command ends automatically when A0 is set to LOW and when the next command is entered.

The 80-series MPU interface starts reading when LOW signal is entered in the $\overline{RD}$ pin, and it starts writing when LOW signal is entered in the $\overline{WR}$ pin. The 68-series MPU starts reading when HIGH signal is entered in the R/$\overline{W}$ pin, and it starts writing when LOW signal is entered in the R/$\overline{W}$ pin. The HIGH signal must be entered in the E pin.

For serial interfacing, data signals are processed as explained in Paragraph 6.1.3.

Any other code not described here must not be used.

7. COMMANDS

7.1 Command List

Table 31 Command List

No.	Command name	Command Code (Hex)	Instruction length (Byte)	Command execution timing	Function
1	Display ON	AF	1	VSYNC	Turns the LCD display ON.
2	Display OFF	AE	1	Immediately afterward	Turns the LCD display OFF.
3	Sets display	CA	10	VSYNC	Number of clocks in 1H and number of display lines Normally white or normally black, etc.
4	Set Display Timing	A1	8	VSYNC	Sets the display timing.
5	Set Data	BC	2	Immediately afterward	RGB array, access direction, built-in oscillator, etc.
6	Set Start Address	15	3	Immediately afterward	Sets the RAM access start address. Start Column Address, Start Row Address
7	Set End Address	75	3	Immediately afterward	Sets the RAM access end address. End Column Address, End Row Address
8	RAM Write	5C	—	Immediately afterward	Writes data into the RAM.
9	RAM Read	5D	—	Immediately afterward	Reads data from the RAM.
10	Read-Modify-Write	E0	—	Immediately afterward	Sets to the read-modify-write state.
11	Set Area Scrolling	AA	5	VSYNC	Sets the area scroll state.
12	Set Display Start Line	AB	2	VSYNC	Starts display of the scrolling area. Set Line Address
13	Partial Display In	A8	4	VSYNC	Sets the partial display state and starts partial display.
14	Partial Display Out	A9	1	VSYNC	Cancels partial display.
15	Set Display Data Interface	31	3	VSYNC	Sets the display data interface.
16	Set Display Color Mode	8B	5	VSYNC	Sets the display color state.
17	Gate Line Scan Mode	6F	4	VSYNC	Sets the gate line scan mode.
18	Set AC Operation Drive	8C	3	VSYNC	Sets the AC operation drive state.
19	Set Electronic Control	20	8	Immediately afterward	Sets the power supply.
20	Set γ Correction Characteristics	22	7	Immediately afterward	Sets the γ correction value.
21	Set Power Control	21	14	VSYNC	Controls the power circuit.
22	Set Partial Power Control	23	8	VSYNC	Controls power supply in partial non-display area.
23	Sleep In	95	1	Immediately afterward	Execute Automatic Off Sequence command
24	Sleep Out	94	1	VSYNC	Execute Automatic On Sequence command

No.	Command name	Command Code (Hex)	Instruction length (Byte)	Command execution timing	Function
25	VOSC OFF	97	1	Immediately afterward	Stops VCORE and VOSC.
26	Turns VOSC ON	96	1	Immediately afterward	Starts up VCORE and VOSC.
27	Stops oscillation	93	1	Immediately afterward	Stops the built-in oscillation circuit.
28	Starts oscillation	92	1	Immediately afterward	Starts the built-in oscillation circuit.
29	Test	FF	8	Immediately afterward	Command for testing
30	NOP	0	1	—	This is the no-operation command that does not affect the system operation.
31	Status Read	E8	3	Immediately afterward	Reads the status.
32	Revision Read	-(E9)	1	Immediately afterward	Reads revision.
33	Soft Reset	99	1	Immediately afterward	Soft Reset

7.2 Initial Values of a Single-Byte Command

Display OFF
Partial Display Out (Normal display)
Sleep In
High-Speed RAM Write Out
VOSC OFF
Stops oscillation.

7.3 Parameter Initial Value List

Table 32 Parameter Initial Value List

No.	Command	Parameter	Code (Bin)								Decimal	Initial state
			D17	D16	D15	D14	D13	D12	D11	D10		
3	Sets display	P1	0	0	0	0	*	*	0	0	0	1H=74 clocks
		P2	0	1	0	0	1	0	0	1	73	1H=74 clocks
		P3	0	0	*	*	*	*	0	0	—	Liquid crystal type, etc.
		P4	*	1	0	0	*	1	0	0	—	Boosting clock frequency
		P5	1	1	0	1	1	0	1	1	219	220-line display
		P6	0	0	0	0	0	0	0	0	0	All pins enabled.
		P7	0	0	0	0	0	0	1	0	2	Number of back poaching lines 3
		P8	0	0	0	0	0	0	0	1	1	Number of front poaching lines 2
		P9	*	*	*	*	*	0	0	0	0	All pins enabled.
4	Set Display Timing	P1	0	0	0	0	0	0	0	0	0	Source output ON at the 1st clock
		P2	0	1	0	0	0	1	1	0	70	Source output OFF at 71st clock
		P3	0	0	0	0	0	1	0	0	4	Gate output ON at the 5th clock
		P4	0	1	0	0	0	1	0	0	68	Gate output OFF at the 69th clock
		P5	*	*	*	*	0	0	0	0	0	Drive mode switch
		P6	0	0	0	1	0	0	1	1	19	V_{COM} boost timing
		P7	0	0	0	0	1	0	0	1	9	Drive mode switch timing
5	Set Data	P1	0	0	0	0	0	0	0	0	—	Row address normal setup
6	Set Start Address	P1	0	0	0	0	0	0	0	0	0	Start Column Address
		P2	0	0	0	0	0	0	0	0	0	Start Row Address
7	Set End Address	P1	1	0	1	0	1	1	1	1	175	End Column Address
		P2	1	1	0	1	1	0	1	1	219	End Row Address
11	Set Area Scrolling	P1	0	0	0	0	0	0	0	0	0	Start address
		P2	1	1	0	1	1	0	1	1	219	End address
		P3	0	0	0	0	0	0	0	0	0	Number of scroll lines 0
		P4	*	*	*	*	*	*	1	1	—	The full-screen can be scrolled.
12	Display Start Line	P1	0	0	0	0	0	0	0	0	0	Display Start Line 0
13	Partial Display In	P1	0	0	0	0	0	0	0	0	0	Area 1 Start Line 0
		P2	0	0	0	0	0	0	0	0	0	Area 1 End Line 0
		P3	0	0	0	0	0	0	0	0	—	Non-display refresh rate
15	Set Display Data Interface	P1	0	0	0	0	0	0	0	0	0	MPU interface 18 bits
		P2	*	*	*	*	*	*	0	0	0	Division is not done.
16	Set Display Color Mode	P1	*	*	*	*	*	0	0	0	—	Select voltage and display color
		P2	*	0	0	1	*	0	0	1	—	Gray scale amplifier ability
		P3	*	1	0	0	*	1	0	0	—	Bias setting
		P4	*	1	0	0	*	1	0	0	—	Boosting clock frequency
17	Set Gate Line Scan Mode	P1	*	*	*	*	0	*	0	0	—	Normal direction, interlace drive
		P2	0	0	0	0	0	0	0	0	0	Scan start line
		P3	1	1	0	1	1	0	1	1	219	Scan end line

No.	Command	Parameter	Code (Bin)								Decimal	Initial state
			D17	D16	D15	D14	D13	D12	D11	D10		
18	Set AC Operation Drive	P1	*	*	*	*	*	*	0	0	—	n-line reverse
		P2	*	*	*	*	0	0	0	0	0	n-line set 1
19	Set Electronic Control	P1	*	*	*	0	0	0	0	0	0	V_{DDHS}
		P2	*	*	0	0	0	0	0	0	0	V_{COMH}
		P3	*	*	*	0	0	0	0	0	0	VCA
		P4	*	*	*	0	0	0	0	0	0	V_{DDRH}
		P5	*	*	*	0	0	0	0	0	0	V_{DDRL}
		P6	*	*	*	0	0	0	0	0	0	V_{ONREG}
		P7	*	*	*	0	0	0	0	0	0	V_{OFREG}
		P8	*	*	*	*	*	0	0	0	0	V_{LDO}
20	Set γ Correction Characteristics	P1	0	0	1	1	0	0	1	0	—	V_{RP3} V_{RP0}
		P2	*	0	0	0	*	0	0	0	—	V_{RP2} V_{RP1}
		P3	*	1	0	0	*	1	0	0	—	V_{P2} V_{P1}
		P4	*	1	0	0	*	1	0	0	—	V_{P4} V_{P3}
		P5	*	1	0	0	*	1	0	0	—	V_{P6} V_{P5}
		P6	*	1	0	0	*	1	0	0	—	V_{P8} V_{P7}
21	Set Power Control	P1	0	0	0	1	0	0	0	0	—	Wait1, 2
		P2	0	0	0	1	0	0	0	1	—	Wait3, 4
		P3	*	*	*	*	0	0	0	0	—	Booster circuit
		P4	0	0	*	0	0	0	0	0	—	Regulator 1
		P5	0	0	0	0	0	0	0	0	—	Regulator 2
		P6	0	0	0	*	*	*	*	*	—	Regulator 3
		P7	*	1	0	0	*	1	0	0	—	Pre-buffer ability setting
		P8	0	0	0	0	0	0	0	0	—	Gray scale amplifier control 1
		P9	*	*	*	*	*	*	0	0	0	Gray scale amplifier control 2
		PA	0	0	0	0	0	0	0	0	0	Gray scale amplifier output Hz1
		PB	*	*	*	*	*	*	0	0	0	Gray scale amplifier output Hz2
		PC	*	0	0	1	*	0	0	1	—	Gray scale amplifier ability
		PD	*	1	0	0	*	1	0	0	—	Bias setting
22	Set Partial Power Control	P1	*	*	*	0	*	0	0	1	—	V_{COM} ability setting
		P2	*	1	0	0	*	1	0	0	—	Boosting clock frequency
		P3	*	*	*	0	0	0	0	0	—	Regulator 1
		P4	0	0	0	*	0	0	0	0	—	Regulator 2
		P5	0	0	0	*	*	*	*	*	—	Regulator 3
		P6	*	0	0	1	*	0	0	1	—	Gray scale amplifier ability
		P7	*	1	0	0	*	1	0	0	—	Bias setting
29	Test	P1	*	*	0	0	0	0	0	0	—	V_{REG} adjustment
		P2	*	*	*	*	0	0	0	0	—	Constant current adjustment
		P3	*	*	*	0	0	0	0	0	—	Oscillation frequency adjustment
		P4	*	0	0	0	0	0	0	0	—	Discharge control 1
		P5	0	0	0	0	0	0	0	0	—	Discharge control 2
		P6	*	*	0	0	0	0	0	0	—	Gate driver test
		P7	0	*	*	*	0	0	0	0	—	Detector test
32	Revision Read	P1	0	0	0	0	1	1	0	1	—	00H

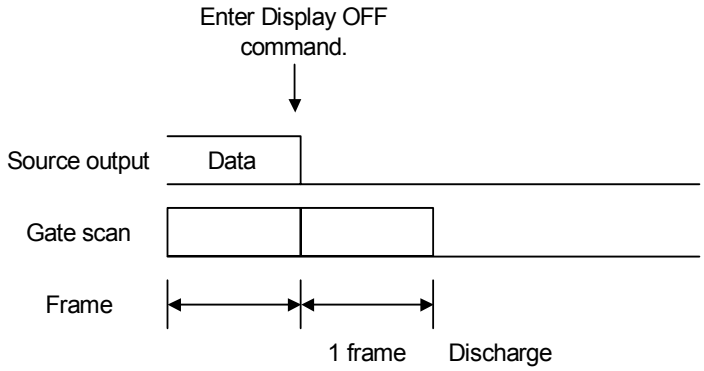
7.4 Explanation of Commands

(1) Display ON (Command code: AFh, Parameter: None)
This command converts the display data stored in the built-in RAM to the gray scale voltage and displays on the LCD panel. The Sleep Out command be entered beforehand. The Display On is waited until it is ready for starting display after Sleep Out. When it is ready, the command is executed.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	1	0	1	1	1	1	Command Display ON

(2) Display OFF (Command code: AEh, Parameter: None)
Turns the LCD display OFF. After receiving the command, display is canceled from the next frame at once.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	1	0	1	1	1	0	Command Display OFF



After receiving the Display OFF command, source output and VCOM output produce an output of VSS and display white (in case of normally white liquid crystal) while turning the gate line on for a period of 1 frame or more. Then, they discharge the power circuits.

(3) Set Display (Command code: CAh, Parameter: 9 bytes)
This command sets the display conditions. P3 and P6 execute immediately. P1, P2, P4, P5, P7 and P8 execute in synchronization with the first VSYNC after P9 was entered.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	1	0	0	1	0	1	0	Set Command Display
P17	P16	P15	P14	*	*	P11	P10	Parameter 1 (P1) Number of clocks in 1H (MSB)
P27	P26	P25	P24	P23	P22	P21	P20	Parameter 2 (P2) Number of clocks in 1H (LSB)
P37	P36	*	*	*	*	P31	P30	Parameter 3 (P3) Liquid crystal type
*	P46	P45	P44	*	P42	P41	P40	Parameter 4 (P4) Sets boosting clock frequency.
P57	P56	P55	P54	P53	P52	P51	P50	Parameter 5 (P5) Number of display dots Y (number of display lines)
P67	P66	P65	P64	P63	P62	P61	P60	Parameter 6 (P6) Source output Hi-Z control
P77	P76	P75	P74	P73	P72	P71	P70	Parameter 7 (P7) Back poaching line
P87	P86	P85	P84	P83	P82	P81	P80	Parameter 8 (P8) Front poaching line
*	*	*	*	*	0	0	0	Parameter 9 (P9) Reserved parameter

Parameter 1 (P1): Sets MSB bits of the number of clocks in 1H and the number of display dots. Sets the expansion MSB bits of front poaching.

P11 to P10: Sets MSB 2 bits of the number of clocks required during 1H (a single-line select period) subtracted by 1.
P17 to P14: Sets MSB 4 bits of the front poaching. (The LSB 8 bits are set by P8).

Parameter 2 (P2): Sets LSB 8 bits of the number of clocks required during 1H (a single-line select period) subtracted by 1. Notice change of the number of clocks of 1H about a relation with display timing set. Please be sure to set up to become longer than the various timing set up by the source timing set. When making a setting value small during display turn ON, it recommends changing display timing set previously.

Example: If the frame frequency is 60Hz, the number of display lines is 220, back poaching is 3 lines, front poaching is 2 lines and the single clock cycle is 1µs:
1 / 60 / (220+2+3) = 74µs (1H)
Set value = 74-1 = 73
P1=00H, P2=49H

Parameter 3 (P3): Sets the address location of RAM and liquid panel type.

P31 and P30: Sets the divided ratio of a built-in oscillation.

P31	P30	Divided ratio
0	0	Non divided (1MHz)
0	1	1/2 (0.5MHz)
1	0	1/4 (0.25MHz)
1	1	Setting disabled

P36: Automatically sets the RAM's column address location linked with the P6 source output Hi-Z.
0: Manual No change of RAM address
1: Automatic Automatically changes the column address location of RAM.

P37: Sets the type of the LCD panel to be used.
0: Normally white
1: Normally black

Parameter 4 (P4): Sets frequency of the boosting clock of the 1st to 4th booster in displaying 262k-color display of display area.

P42 to P40: Sets frequency of the boosting clock of the 1st and 2nd boosters in displaying 262k-color display.
P46 to P44: Sets frequency of the boosting clock of the 3rd and 4th boosters in displaying 262k-color display.
Determine while checking the display.

P42/P46	P41/P45	P40/P44	Frequency
0	0	0	= Stop (disable)
0	0	1	= Frequency in 1H × 8
0	1	0	= Frequency in 1H × 4
0	1	1	= Frequency in 1H × 2
1	0	0	= Frequency in 1H × 1
1	0	1	= Frequency in 1H / 2
1	1	0	= Frequency in 1H / 4
1	1	1	= Frequency in 1H / 8

Parameter 5 (P5): Sets the number of dots to be displayed in the direction of Y subtracted by 1. Odd lines cannot be set up.
Example) To use a 176RGB × 220-dot LCD panel:
Set value = 220-1 = 219

Parameter 6 (P6): Sets source output not to be used to Hi-Z. Sets a maximum of 16 outputs to Hi-Z and allows 160-dot display.

P63	P62	P61	P60	Pins set to Hi-Z
0	*	*	*	All pins enabled
1	0	0	0	S1-S3
1	0	0	1	S1-S6
1	0	1	0	S1-S9
1	0	1	1	S1-S12
1	1	0	0	S1-S15
1	1	0	1	S1-S18
1	1	1	0	S1-S21
1	1	1	1	S1-S24

P67	P66	P65	P64	Pins set to Hi-Z
0	*	*	*	All pins enabled
1	0	0	0	S528-S526
1	0	0	1	S528-S523
1	0	1	0	S528-S520
1	0	1	1	S528-S517
1	1	0	0	S528-S514
1	1	0	1	S528-S511
1	1	1	0	S528-S508
1	1	1	1	S528-S505

Parameter 7 (P7): Sets the number of lines for back poaching subtracted by 1.
P77 to P70: Sets the number of lines for back poaching in the range from 1 to 256.
It recommends that is making a change of the number of lines before sleep out. When it changes during display turn on, a display may be abnormal a moment. Since it may be VCOM is same voltage potential 2-frame period. (Attention follows coincidence becomes abnormal. Odd lines to even lines and even lines to odd lines. Odd lines to odd lines and even lines to even lines are not happen)

Parameter 8 (P8): Sets the number of lines of front poaching subtracted by 1.
P87 to P80: Sets the number of lines for front poaching in the range from 2 to 4096 by combining with MSB 4

bits of P1. 1 line (00h) is prohibition of a setup.

Parameter 9 (P9): Test parameter Specify 000.
P92 to 90: Specifying 1 sets all source outputs to Hi-Z.

(4) Set Display Timing (Command code: A1h, Parameter: 7 bytes)
With the clock setting of the display timing, the output timing best-suited to the characteristics of the panel to be connected can be obtained.

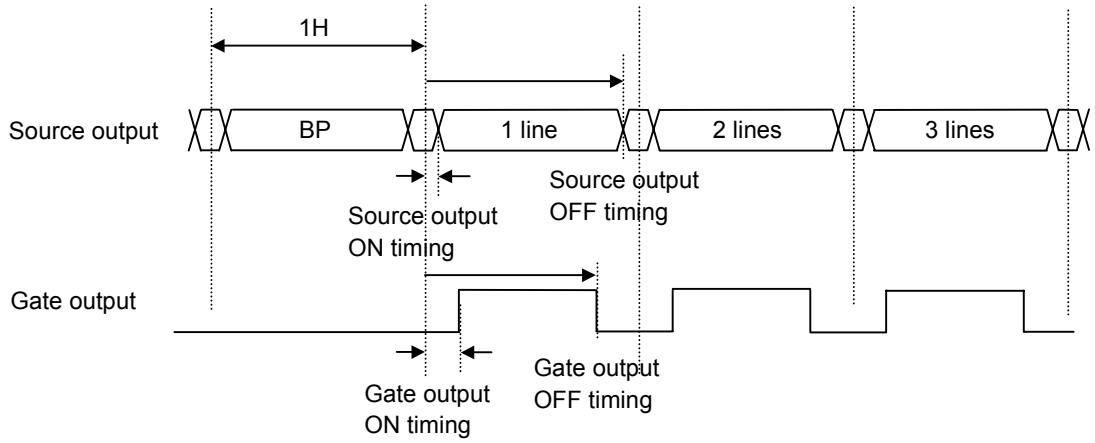


Fig.46 Display Timing Control

Enable the source output (S1 to S528 pins) and set the timing of Hi-Z and ON/OFF timing of the LCD output of the gate driver. Set the timing within the range of the number of clocks required during 1H (a single-line select period) subtracted by 1, which was set by 0 - Set Display P1. Set the timing to be changed subtracted by 1.
It is the number of clocks of the oscillator when using the built-in oscillator for the display timing, or the number of DOTCLKs when using the DOTCLK. It becomes the DOTCLK number that was divided in the case that it divided with P2 of the display data interface set.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	1	0	0	0	0	1	Command Set Display Timing
P17	P16	P15	P14	P13	P12	P11	P10	Parameter 1 (P1) Source Output ON Timing
P27	P26	P25	P24	P23	P22	P21	P20	Parameter 2 (P2) Source Output OFF Timing
P37	P36	P35	P34	P33	P32	P31	P30	Parameter 3 (P3) Gate Signal “Select” Timing
P47	P46	P45	P44	P43	P42	P41	P40	Parameter 4 (P4) Gate Signal “Non-select” Timing
*	*	*	*	P53	P52	P51	P50	Parameter 5 (P5) Sets selection of drive mode
P67	P66	P65	P64	P63	P62	P61	P60	Parameter 6 (P6) V_{COMH} and V_{COML} boost timing
P77	P76	P75	P74	P73	P72	P71	P70	Parameter 7 (P7) Sets the switching timing of drive mode

Parameter 1 (P1): Sets the turn-ON (enabling) timing of source outputs (S1 to S528 pins) to the number of clocks from the beginning of the line subtracted by 1.

Parameter 2 (P2): Sets the turn-OFF (Hi-Z) timing of source outputs (S1 to S528 pins) to the number of clocks from the beginning of the line subtracted by 1.
It sets up so that it may surely become source on timing < source off timing. Moreover, it is necessary to set up source of timing by the less than -2 CK number of 01h to 1H.

Parameter 3 (P2): Sets the turn-ON (V_{DDHG}) timing of gate outputs (G1 to G220 pins) to the number of clocks from the beginning of the line subtracted by 1.

Parameter 4 (P4): Sets the turn-OFF (V_{EE}) timing of gate outputs (G1 to G220 pins) to the number of clocks from the beginning of the line subtracted by 1.

It sets up so that it may surely become gate on timing < gate off timing. Moreover, it is necessary to set up gate of timing by the less than -1 CK number of 01h to 1H.

Parameter 5 (P5): Selects the source drive mode, power down for the gray scale generation circuit after the source output Hi-Z and the V_{COMH} and V_{COML} ability control.

P53: Selects whether or not to UP (boost) the ability of V_{COMH} and V_{COML}. The boosting timing is set by P6. This command is valid when power control command of P56 sets to 1.
0: Not boost
1: Boost

P52: Selects whether or not to enable power saving of the gray scale voltage generation circuit after the source OFF timing.
0: Not enable power saving
1: Enable power saving

P52 generally uses not to power save. Power-save may be used to reduce power by decreasing the frame frequency. Carefully check the indication before using it.

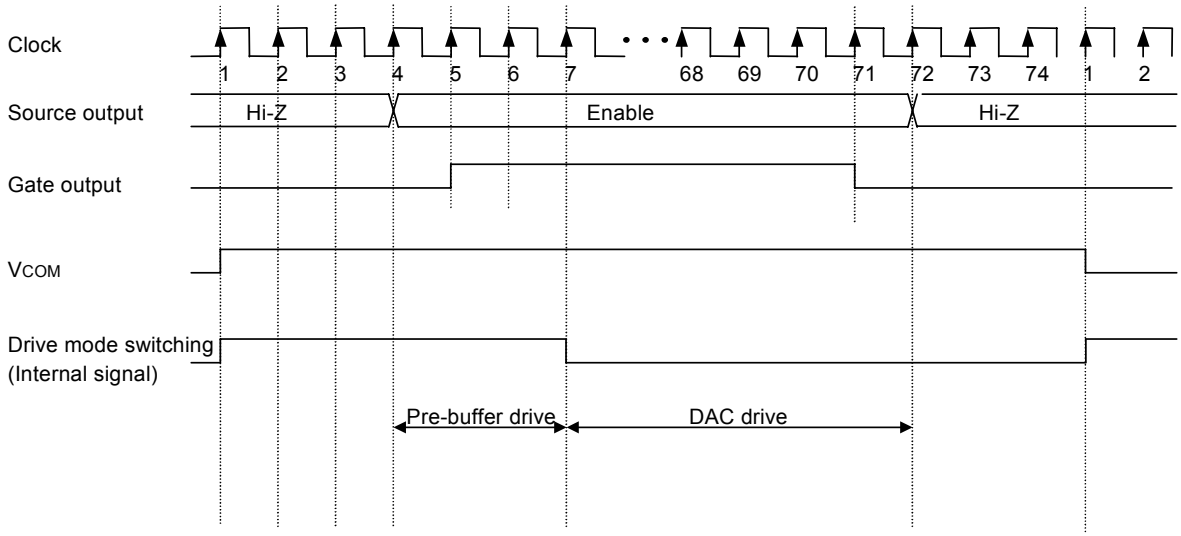
P51 and P50: Select the source drive mode.

P51	P50	Switch mode
0	0	Switches between pre-buffer drive and centralized DAC drive at the timing set by P7.
0	1	Centralized DAC drive throughout the period of source output enable. P7 is ignored.
1	0	Pre-buffer drive throughout the period of source output enable. P7 is ignored.
1	1	Setting disabled

Parameter 6 (P6): With P67 to P60, sets the timing of bringing UP (boost) the ability of the regulator of the built-in power supply to the number of clocks from the beginning of the line subtracted by 1. If it is being boosted by the Power Control command, the above setting is invalid.

Parameter 7 (P7): With P77 to P70, sets the timing of switching between pre-buffer drive and centralized DAC drive to the number of clocks from the beginning of the line subtracted by 1.
In pre-buffer + concentration DAC drive (P51, P50= 0,0), change timing is surely set as source ON timing <P7< source OFF timing. Moreover, in any drive systems, 00h is prohibition of a setup.

Setup Example
Source Output On Timing P1 = 3
Source Output Off Timing P2 = 71
Gate Signal Select Timing P3 = 4
Gate Signal Non-select Timing P4 = 70
Source Drive Mode, etc. P5 = 00
VCOMH and VCOML Boost Timing P6 = 19 (invalid)
Drive Mode Switching Timing P7 = 6 (P51, P50 = 0, 0)



(5) Set Data (Command code: BCh, Parameter: 1 byte)
Sets display data conditions. Change the display RAM address direction and the scan direction while the Display OFF is set, and wait for 1ms or more after changing. When only parameters not related to the display RAM are changed, the setting is immediately enabled. In this case, there is no need to wait.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	1	1	1	1	0	0	Command Set Data
P17	P16	P15	P14	P13	P12	P11	P10	Parameter 1 (P1) Controls built-in oscillator

Parameter 1 (P1)

P10: Row address normal/reverse
0: Normal
1: Reverse

P11: Column address normal/reverse
0: Normal (S1 to 3: Address 0, S526 to S528: Address 175)
1: Reverse (S1 to 3: Address 175, S526 to S528: Address 0)

P12: Selects oscillation clock output built into the OSCO pin
Usually, it is used by Hi-Z. When making it output, It recommends connecting the capacitor of 1uF to VOSC pin.
0: Hi-Z
1: Output

P13: Selects the address scan direction when display data is written into (or read from) the RAM from the MPU interface. When the RGB interface is used, select "Incremented when written (or read) in the column address direction".
0: Incremented when written (or read) in the column address direction.
1: Incremented when written (or read) in the row address direction.

P14: Sets the assignment order of RGB corresponding to the order of S1, S2, S3….pins.
0: RGB (S1:R S2:G S3:B・・・S528:B)
1: BGR (S1:B S2:G S3:R・・・S528:R)

P15: Selects the number of bits of display data when display data is written into (or read from) the RAM when the MPU interface is 16-bit parallel.
0: 16 bits × 1 time
1: 16 bits × 2 times

With P16:15, select each data format of the 1st and 2nd transfer when set to 16 bits × two times.
0: 1st transfer 2 bits, 2nd transfer 16 bits
1: 1st transfer 16 bits, 2nd transfer 2 bits

P17: Selects oscillator.
0: Uses the built-in oscillator.
1: Does not use the built-in oscillator (but enters external clocks via the OSCI pin. It is an object for a test.)

(6) Set Start Address (Command code: 15h, Parameter: 2 bytes)
Sets the access start address of the display RAM.

D17	D16	D15	D14	D13	D12	D11	D10	Function
0	0	0	1	0	1	0	1	Command Set Start Address
P17	P16	P15	P14	P13	P12	P11	P10	Parameter 1 (P1) Column Address
P27	P26	P25	P24	P23	P22	P21	P20	Parameter 2 (P2) Row Address

P17	P16	P15	P14	P13	P12	P11	P10	Column address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
			:					:
1	0	0	0	1	1	1	0	AEH
1	0	1	0	1	1	1	1	AFH

P27	P26	P25	P24	P23	P22	P21	P20	Row address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
			:					:
1	0	1	0	1	1	1	0	DAH
1	1	0	1	1	0	1	1	DBH

(7) Set End Address (Command code: 75h, Parameter: 2 bytes)
Sets the access end address of the display RAM. After receiving the command, the setting is enabled immediately.

D17	D16	D15	D14	D13	D12	D11	D10	Function
0	1	1	1	0	1	0	1	Command Set End Address
P17	P16	P15	P14	P13	P12	P11	P10	Parameter 1 (P1) Column Address
P27	P26	P25	P24	P23	P22	P21	P20	Parameter 2 (P2) Row Address

The setting range is the same as the start address. However, the start address < the end address must be true.

(8) RAM Write (Command code: 5Ch, Parameter: unlimited)
Automatically increments the address based on the $\overline{WR}$ signal after command input, and writes parameters as the data into the display data RAM. When a command is entered, the column and row addresses are set to their start address. Any number of bytes of parameters can be written until the next command is entered. When the write address reaches the end address, it is returned to the start address.
The relationship between the parameter (display data) bit length and pins varies depending on the interface used as described in 6.2.3.

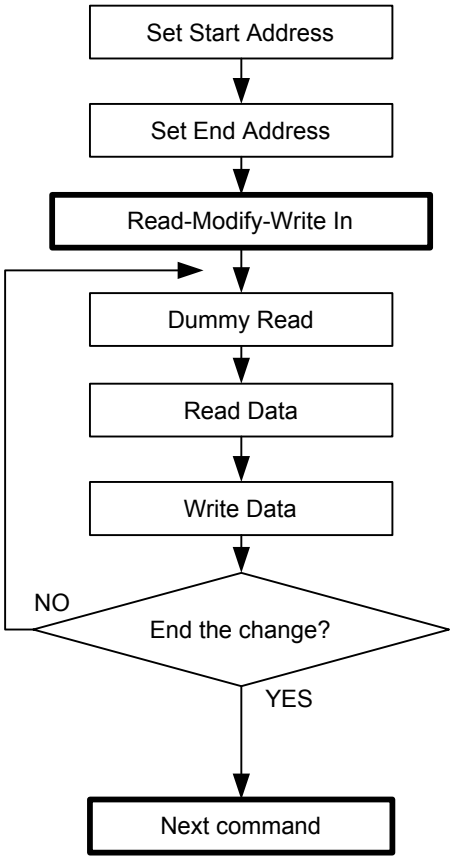
D17	D16	D15	D14	D13	D12	D11	D10	Function
0	1	0	1	1	1	0	0	Command RAM Write
*	*	*	*	*	*	*	*	Parameter Specifies data to be written into the display RAM.

(9) RAM Read (Command code: 5Dh, Parameter: unlimited)
Automatically increments the address based on the $\overline{RD}$ signal after command input, and reads data from the display RAM. When a command is entered, the column and row addresses are set to their start address. The data reading is continued until the next command is entered. Any number of bytes of data can be read. When the read address reaches the end address, it is returned to the start address.
The relationship between the parameter (display data) bit length and pins varies depending on the interface used as described in 6.2.3.

D17	D16	D15	D14	D13	D12	D11	D10	Function
0	1	0	1	1	1	0	1	Command RAM Read
*	*	*	*	*	*	*	*	Parameter Specifies data to be read from the display RAM

(10) Read-Modify-Write (Command code: E0h, Parameter: unlimited)
This command makes both RAM Write and RAM Read executable and reduces the CPU load when the RAM area data is repeated to change. If the memory is set to the Read-Modify-Write status by the Read-Modify-Write command, the addresses are NOT incremented automatically by the read signal ($\overline{RD}$ for 80-series) until it is released. It is incremented only by the write signal ($\overline{WR}$ for 80-series). This state is canceled when another command is entered. When the Read-Modify-Write status is released, control is returned to the address specified by the Set Start Address command before status change.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	1	1	0	0	0	0	0	Command Read-Modify-Write



(11) Set Area Scrolling (Command code: AAh, Parameter: 4 bytes)
Makes settings for partially scrolling the screen in the row direction. With this command and the following 4 parameters, type of area scroll, fixed area and scroll area can be set.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	1	0	1	0	1	0	Command Set Area Scrolling
P17	P16	P15	P14	P13	P12	P11	P10	Parameter 1 (P1) Scroll Start Line Address
P27	P26	P25	P24	P23	P22	P21	P20	Parameter 2 (P2) Scroll End Line Address
P37	P36	P35	P34	P33	P32	P31	P30	Parameter 3 (P3) Number of Scroll Lines
*	*	*	*	*	*	P41	P40	Parameter 4 (P4) Scroll Mode

Parameter (P1): Specifies the scroll start line address of the RAM to be assigned to the scroll area. For top area and the full-screen scrolling, set it to the 0 address. The display start line address is also set to this scroll start line address until it is set with the Display Start Line command.

Parameter 2 (P2): Specifies the scroll end line address of the RAM to be assigned to the scroll area. For bottom area and the full-screen scrolling, set it to the 219 addresses. Keep the scroll start line address < scroll end line address true.

Parameter 3 (P3): Sets the value to the number of scroll lines.
Sets the value to the number of display lines (set by P3 of Set Display) subtracted by the number of display lines in the bottom fixed area. For the bottom area and the full-screen scrolling, set it to any value (the set value is ignored).

Parameter (P4): Selects an area scroll mode.

P41	P40	Area scroll type
0	0	The center area can be scrolled
0	1	The top area can be scrolled
1	0	The bottom area can be scrolled
1	1	The full-screen can be scrolled

An area can be scrolled only after the Set Area Scroll command has been issued and the display start address has been set by the Display Start Line command.

[Area scroll setup example]
Conditions: Set the number of display lines to 220 and scroll the center window. Also, select 16 lines for the top fixed area and 8 lines for the bottom fixed area.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	1	0	1	0	1	0	Set Area Scrolling
0	0	0	1	0	0	0	0	Scroll start address (16)
1	1	1	0	1	1	1	1	Scroll end address (219 - 8 = 211)
1	1	0	0	0	1	1	1	Number of scroll lines (219 - 8 = 211)
*	*	*	*	*	*	0	0	Scroll mode

(12) Set Display Start Line (Command code: ABh, Parameter: 1 byte)
Sets the display start line address of the display RAM. From the scroll area addresses specified by this command, select the display start address. If this command is repeated in a certain cycle, the window can be scrolled dynamically.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	1	0	1	0	1	1	Command Set Display Start Line
P17	P16	P15	P14	P13	P12	P11	P10	Parameter Display start line address

(13) Partial Display In (Command code: A8h, Parameter: 3 bytes)
Used to partially display the screen (by line division) to reduce the power consumption.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	1	0	1	0	0	0	Command Partial In
P17	P16	P15	P14	P13	P12	P11	P10	Parameter 1 (P1) Partial Display Start Line
P27	P26	P25	P24	P23	P22	P21	P20	Parameter 2 (P2) Partial Display End Line
P37	P36	P35	P34	P33	P32	P31	P30	Parameter 3 (P3) Frame frequency in the non-display area

From the number of display lines specified by parameter P3 of the Set Display command, set the partial display address using P1 and P2. (It is NOT the line address. It is the display line of the panel, beginning from line number 0. See below.) P3 sets the number of off voltage write frames during the period of the partial non-display and the partial type.

Line 1
Line 2
Line 3
Line 4
•••
Line 219
Line 220

When the number of display lines is 220

Parameter 1 (P1): Specifies the partial display start line number subtracted by 1 of the above line.
Example: To start partial display at line 1, specify 0.
To start partial display at line 4, specify 3.

Parameter 2 (P2): Specifies the partial display end line number subtracted by 1 of the above line.
Example: To end partial display at line 15, specify 14.

Parameter 3 (P3): Sets the non-display area refresh rate and drive voltage at the time of refreshment.

P36 to 30: Sets the frame frequency that refreshes the partial non-display area to 1/N in the display area. For both source and common, the drive voltage when not refreshed is set to Hi-Z state.

0000000 : 1
0000001 : 1/3
0000010 : 1/5
0000011 : 1/7
•
1111110 : 1/253
1111111 : Does not refresh

P37: Switches mode between V_{DDHS}/V_{SS} mode and V_0/V_{63} mode. Since no gray scale amplifier is used in V_{DDHS}/V_{SS} mode, power consumption is lowered. In V_0/V_{63} mode, display with less power used is also possible, because the gray scale amplifier that generates V_1 to V_{62} gray scale voltage is stopped.

0: Sets to V_{DDHS}/V_{SS} mode.
1: Sets to V_0/V_{63} mode.

(14) Partial Display Out (Command code: A9h, Parameter: None)
The Partial Out command cancels the partial display and returns to the normal display mode. After receiving the command, the setting is enabled from the next frame.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	1	0	1	0	0	1	Command Partial Display Out

(15) Set Display Data Interface (Command code: 31h, Parameter: 1 byte)
Sets the operation state of the display interface. After receiving the command, the setting is enabled immediately.

D17	D16	D15	D14	D13	D12	D11	D10	Function
0	0	1	1	0	0	0	1	Command Set Display Data Interface
P17	P16	P15	P14	P13	P12	P11	P10	Parameter 1 (P1) Sets display interface
*	*	*	*	*	P22	P21	P20	Parameter 2 (P2) Dividing ratio of DOTCLK

Parameter 1 (P1): Sets the operation mode and bus width of the display interface.
P12 to P10:

P12	P11	P10	Data transfer mode
0	0	0	Normal MPU data transfer
0	0	1	
0	1	1	VSYNC Interface
1	0	0	RGB transfer 1
1	0	1	RGB transfer 2
1	1	1	RGB transfer 3
*	1	0	Setting disabled

The period beyond 1H is required for the change of a display interface between the last display line and VSYNCI.

P13 0: At the rising edge of the DOTCLK, data is read.
1: At the falling edge of the DOTCLK, data is read.

P15, P14:

P15	P14	RGB interface bus width
0	0	18 bits (1 dot transferred in 1 step)
0	1	16 bits (1 dot transferred in 1 step)
1	0	6 bits (1 dot transferred in 3 steps)
1	1	Setting disabled

P16: ENABLE
0: LOW enabled.
1: HIGH enabled.

P17: HSYNC, VSYNC
0: LOW enabled.
1: HIGH enabled.

Parameter 2 (P2): Determines the dividing ratio of DOTCLK.
If the display RAM is written at a high speed using DOTCLK as display clock, the display timing may not be set properly. In this case, set the division ratio to specify an appropriate value for the display timing. The clock to be set for each command parameter is a clock after division. The count value of division is reset at the beginning of each line.

P22	P21	P20	Division ratio
0	0	0	Division is not done.
0	0	1	1/2 division
0	1	0	1/3 division
0	1	1	1/4 division
1	0	0	1/5 division
1	0	1	1/6 division
1	1	0	1/7 division
1	1	1	1/8 division

(16) Set Display Color Mode (Command code: 8Bh, Parameter: 4 bytes)
Sets the maximum number of display colors. After receiving the command, the setting is enabled from the next frame.
Switching between 262K-color mode and 8-color mode is available using the Set Display Color Mode command parameter. Only the MSB in the display RAM is used as the gray scale data used for display.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	0	0	1	0	1	1	Command Set Display Color Mode
*	*	*	*	*	P12	P11	P10	Parameter 1 (P1) Maximum number of display color
*	P26	P25	P24	*	P22	P21	P20	Parameter 2 (P2) Sets gray scale amplifier ability
*	P36	P35	P34	*	P32	P31	P30	Parameter 3 (P3) Sets bias circuit ability
*	P46	P45	P44	*	P42	P41	P40	Parameter 4 (P4) Sets the boosting frequency.

Parameter 1 (P1):

P11, 10: Switches mode between V_{DDHS}/V_{SS} mode and V_0/V_{63} mode. Since no gray scale amplifier is used in V_{DDHS}/V_{SS} mode, power consumption is lowered. In V_0/V_{63} mode, display with less power used is also possible, because the gray scale amplifier that generates V_1 to V_{62} gray scale voltage is stopped.
P10: 0 Specifies 8-color V_{DDHS}/V_{SS} mode when P11 is set to 1. It is invalid when P11 is set to 0.
P10: 1 Specifies 8-color V_0/V_{63} mode when P11 is set to 1. It is invalid when P11 is set to 0.
P11:0 Sets the maximum number of display colors to 262K colors.
P11:1 Sets the maximum number of display colors to 8 colors.
P12: Sets whether or not to boost V_{COMH} and V_{COML} in the 8-color-display area similarly to P53 (boosting of V_{COMH} and V_{COML}) of Set Display Timing.
0: Not boost
1: Boost

Parameter 2 (P2) to Parameter 3 (P3): Sets power control of the 8-color display. It is valid only when P11 = 1.

Parameter 2 (P2): See PC of power control.

Parameter 3 (P3): See PD of power control.

Parameter 4 (P4): Sets frequency of the boosting clock of the 1st - 4th booster in 8-color display area.

P42 to P40: Sets frequency of the boosting clock of the 1st and 2nd boosters in the 8-color display area.
P46 to P44: Sets frequency of the boosting clock of the 3rd and 4th boosters in the 8-color display area.
Determine while checking the display.

P42, P46	P41, P45	P40, P44	Frequency

0	0	0	= Stop (disable)
0	0	1	= Frequency in 1H × 8
0	1	0	= Frequency in 1H × 4
0	1	1	= Frequency in 1H × 2
1	0	0	= Frequency in 1H × 1
1	0	1	= Frequency in 1H / 2
1	1	0	= Frequency in 1H / 4
1	1	1	= Frequency in 1H / 8

(17) Set Gate Line Scan Mode (Command code: 6Fh, Parameter: 3 bytes)
Sets the line scan mode of the gate driver.
Be sure to enter before the Sleep Out command.

D17	D16	D15	D14	D13	D12	D11	D10	Function
0	1	1	0	1	1	1	1	Command Set Gate Line Scan Mode
*	*	*	*	P13	*	P11	P10	Parameter 1 (P1) Scan Mode
P27	P26	P25	P24	P23	P22	P21	P20	Parameter 2 (P2) Number of Scan Start Line
P37	P36	P35	P34	P33	P32	P31	P30	Parameter 3 (P2) Number of Scan End Line

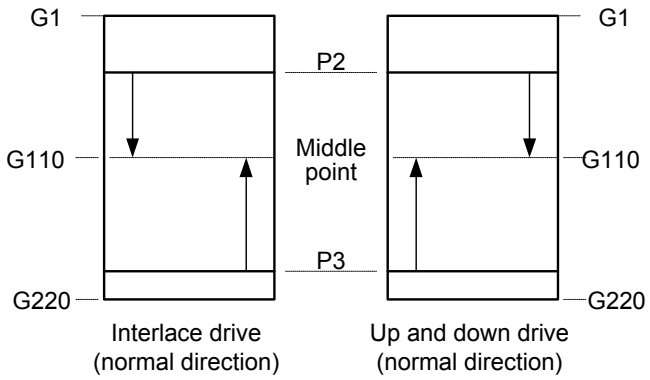
Parameter 1 (P1): Sets the gate line scan mode.

P11	P10	Mode
0	0	Interlace drive
0	1	Up and down drive 1
1	0	Up and down drive 2
1	1	Setting disabled

P13: 0 Normal direction scan
1 Reverse direction scan

Parameter 2 (P2): Sets the gate scan start line subtracted by 1.

Parameter 3 (P3): Sets the gate scan end line subtracted by 1.



It needs to be completely in agreement with P5 (the number of display dots) of display set command. It cannot respond to the panel of odd lines. Refer to the 6.6th clause for the details about the setting method.

(18) Set AC Operation Drive (Command code: 8Ch, Parameter: 2 bytes)
Sets the AC operation drive state. After receiving the command, the setting is enabled from the next frame.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	0	0	1	1	0	0	Command Set AC Operation Drive
*	*	*	*	*	*	P11	P10	Parameter 1 (P1) AC operation mode
*	*	*	*	P23	P22	P21	P20	Parameter 2 (P2) n-line reverse

Parameter 1 (P1): Sets the AC operation mode.

P11	P10	AC operation mode
0	0	n-line reverse driving
0	1	Frame reverse driving
1	0	Interlace drive
1	1	Setting disabled

Parameter 2 (P2): Sets the number of lines for n-line reverse driving subtracted by 1.

(19) Set Electronic Control (Command code: 20h, Parameter: 7 bytes)
Determines the output voltage of each voltage regulator of the built-in power circuit.

D17	D16	D15	D14	D13	D12	D11	D10	Function
0	0	1	0	0	0	0	0	Command Set Electronic Control
*	*	*	P14	P13	P12	P11	P10	Parameter 1 (P1) VDDHS
*	*	P25	P24	P23	P22	P21	P20	Parameter 2 (P2) VCOMH
*	*	*	P34	P33	P32	P31	P30	Parameter 3 (P3) VCA, VCOMW
*	*	*	P44	P43	P42	P41	P40	Parameter 4 (P4) VONREG
*	*	*	P54	P53	P52	P51	P50	Parameter 5 (P5) VOFREG
*	*	*	P64	P63	P62	P61	P60	Parameter 6 (P6) VDDRH
*	*	*	P74	P73	P72	P71	P70	Parameter 7 (P7) VDDRL
*	*	*	*	*	P82	P81	P80	Parameter 7 (P8) VLDO

Parameter 1 (P1) to Parameter 7 (P8): Sets the output voltage of each voltage reagulator.

EVR	VCOMH	VDDHS	VDDRH	VOFREG	VCOMW	VCA	VONREG	VDDRL	VLDO
0	2	2.7	2.7	2	3.0	1.5	0.0	0	3
1	2.075	2.8	2.8	2.1	3.1	1.55	0.2	0.05	2.95
2	2.15	2.9	2.9	2.2	3.2	1.6	0.4	0.1	2.9
3	2.225	3	3	2.3	3.3	1.65	0.6	0.15	2.8
4	2.3	3.1	3.1	2.4	3.4	1.7	0.8	0.2	2.7
5	2.375	3.2	3.2	2.5	3.5	1.75	1.0	0.25	2.6
6	2.45	3.3	3.3	2.6	3.6	1.8	1.2	0.3	2.55
7	2.525	3.4	3.4	2.7	3.7	1.85	1.4	0.35	2.5
8	2.6	3.5	3.5	2.8	3.8	1.9	1.6	0.4	
9	2.675	3.6	3.6	2.9	3.9	1.95	1.8	0.45	
10	2.75	3.7	3.7	3	4.0	2	2.0	0.5	
11	2.825	3.8	3.8	3.1	4.1	2.05	2.2	0.55	
12	2.9	3.9	3.9	3.2	4.2	2.1	2.4	0.6	
13	2.975	4	4	3.3	4.3	2.15	2.6	0.65	
14	3.05	4.1	4.1	3.4	4.4	2.2	2.8	0.7	
15	3.125	4.2	4.2	3.5	4.5	2.25	3.0	0.75	
16	3.2	4.3	4.3	3.6	4.6	2.3	3.2	0.8	
17	3.275	4.4	4.4	3.7	4.7	2.35	3.4	0.85	
18	3.35	4.5	4.5	3.8	4.8	2.4	3.6	0.9	
19	3.425	4.6	4.6	3.9	4.9	2.45	3.8	0.95	
20	3.5	4.7	4.7	4	5.0	2.5	4.0	1	
21	3.575	4.8	4.8	4.1	5.1	2.55	4.2	1.05	
22	3.65	4.9	4.9	4.2	5.2	2.6	4.4	1.1	
23	3.725	5	5	4.3	5.3	2.65	4.6	1.15	
24	3.8	5.1	5.1	4.4	5.4	2.7	4.8	1.2	
25	3.875	5.2	5.2	4.5	5.5	2.75	5.0	1.25	
26	3.95	5.3	5.3	4.6	5.6	2.8	5.2	1.3	
27	4.025	5.4	5.4	4.7	5.7	2.85	5.4	1.35	
28	4.1	5.5	5.5	4.8	5.8	2.9	5.6	1.4	
29	4.175	5.6	5.6	4.9	5.9	2.95	5.8	1.45	
30	4.25	5.7	5.7	5	6.0	3	6.0	1.5	
31	4.325	5.8	5.8	5.1	6.1	3.05	6.2	1.55	

EVR	VCOMH
32(20h)	4.4
33(21h)	4.475
34(22h)	4.55
35(23h)	4.625
36(24h)	4.7
37(25h)	4.775
38(26h)	4.85
39(27h)	4.925
40(28h)	5
41(29h)	5.075
42(2Ah)	5.15
43(2Bh)	5.225
44(2Ch)	5.3
45(2Dh)	5.375
46(2Eh)	5.45
47(2Fh)	5.525
48(30h)	5.6
49(31h)	5.675
50(32h)	5.75
51(33h)	5.825
52(34h)	5.9
53(35h)	5.975
54(36h)	5.975
55(37h)	5.975
56(38h)	5.975
57(39h)	5.975
58(3Ah)	5.975
59(3Bh)	5.975
60(3Ch)	5.975
61(3Dh)	5.975
62(3Eh)	5.975
63(3Fh)	5.975

The above values are calculated values only and no guarantee on them is offered. In reality, since computations are performed based on VREG and output to the regulator, variations in VREG and regulators are included.
For VCOMH, the output voltage can be adjusted with the external resistor. There is connection way that can be half voltage of VCOMW.

(20) Set γ Correction Characteristics (Command code: 22h, Parameter: 12 bytes)
Sets gray scale voltage according to the γ characteristics of the LCD panel.

D17	D16	D15	D14	D13	D12	D11	D10	Function
0	0	1	0	0	0	1	0	Command Set γ Correction Characteristics
P17	P16	P15	P14	P13	P12	P11	P10	Parameter 1 (P1) V_{RP3} V_{RP0}
*	P26	P25	P24	*	P22	P21	P20	Parameter 2 (P2) V_{RP2} V_{RP1}
*	P36	P35	P34	*	P32	P31	P30	Parameter 3 (P3) V_{P2} V_{P1}
*	P46	P45	P44	*	P42	P41	P40	Parameter 4 (P4) V_{P4} V_{P3}
*	P56	P55	P54	*	P52	P51	P50	Parameter 5 (P5) V_{P6} V_{P5}
*	P66	P65	P64	*	P62	P61	P60	Parameter 6 (P6) V_{P8} V_{P7}

Parameter 1 (P1): Positive polarity side tilt adjustment register V_{RP3} and V_{RP0}

Parameter 2 (P2): Positive polarity side tilt adjustment register V_{RP2} and V_{RP1}

Parameter 3 (P3): Positive polarity side fine adjustment selector V_{P2} and V_{P1}

Parameter 4 (P4): Positive polarity side fine adjustment selector V_{P4} and V_{P3}

Parameter 5 (P5): Positive polarity side fine adjustment selector V_{P6} and V_{P5}

Parameter 6 (P6): Positive polarity side fine adjustment selector V_{P8} and V_{P7}

Setting the positive polarity automatically sets the negative polarity to be symmetrical.
For details on how to set, see section 6.11 “Gray scale Voltage Generation Circuit”.

(21) Set Power Control (Command code: 21h, Parameter: 13 bytes)
Sets ON or OFF of a function and ability of power circuit. The setup is performed automatically and sequentially with the Sleep Out command in accordance with the setting of this command.

D17	D16	D15	D14	D13	D12	D11	D10	Function
0	0	1	0	0	0	0	1	Command Set Power Control
P17	P16	P15	P14	P13	P12	P11	P10	Parameter 1 (P1) Wait 1 and 2 (Sleep Out)
P27	P26	P25	P24	P23	P22	P21	P20	Parameter 2 (P2) Wait 3 and 4 (Sleep Out)
*	*	*	*	P33	P32	P31	P30	Parameter 3 (P3) Booster circuit control, etc.
P47	P46	*	P44	P43	P42	P41	P40	Parameter 4 (P4) Regulator circuit control 1
P57	P56	P55	P54	P53	P52	P51	P50	Parameter 5 (P5) Regulator circuit control 2
P67	P66	P65	*	*	*	*	*	Parameter 6 (P6) Regulator circuit control 3
*	P76	P75	P74	*	P72	P71	P70	Parameter 7 (P7) Sets pre-buffer ability
P87	P86	P85	P84	P83	P82	P81	P80	Parameter 8 (P8) Gray scale amplifier control 1
*	*	*	*	*	*	P91	P90	Parameter 9 (P9) Gray scale amplifier control 2
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Parameter A (PA) Gray scale amplifier output Hz1
*	*	*	*	*	*	PB1	PB0	Parameter B (PB) Gray scale amplifier output Hz2
*	PC6	PC5	PC4	*	PC2	PC1	PC0	Parameter C (PC) Sets gray scale amplifier ability
*	PD6	PD5	PD4	*	PD2	PD1	PD0	Parameter D (PD) Sets bias circuit ability

Parameter 1 (P1): Sets Wait 1 or 2 during Sleep Out

Parameter 2 (P2): Sets Wait 3 or 4 during Sleep Out
P10 to P13: Wait 1
P14 to P17: Wait 2
P20 to P23: Wait 3
P24 to P27: Wait 4

0000: No wait
0001: 1 frame
0010: 2 frames
•
1111: 15 frames

Parameter 3 (P3): P33 to P30 booster circuit V_{LDO} ON/OFF control
P30: 0 V_{LDO} OFF
: 1 V_{LDO} ON

0: Booster circuit OFF
1: Booster circuit ON
P31: 1st and 2nd booster circuit
P32: 3rd booster circuit
P33: 4th booster circuit

Parameter 4 (P4): Regulator circuit ON/OFF control 1
0: Regulator OFF
1: Regulator ON (Cancels discharge and turns the regulator ON.)
P40: V_{DDHS}
P41: V_{OFREG}
P42: V_{ONREG}
P43: V_{DDRH}
P44: V_{DDRL}

P47, P46: Sets the reference voltage. Sets to VREG1.

P47	P46	Reference voltage	VREG Voltage	Setting
0	0	VREG1	3.5V	Valid
0	1	VREG2	3.5V	Setting disabled
1	0	VREG3	3.5V	Setting disabled
1	1	Setting disabled	-	Setting disabled

Parameter 5 (P5): Regulator circuit ON/OFF control 2
0: Regulator OFF
1: Regulator ON (Cancels discharge and turns the regulator ON.)
P50: VCOMH
P51: Set to 0.
P52: VCOML
P53: VCOM
For testing.

P54: Fixes at 0 (Resistor built into VCOMH is ON.)

VCOMH and VCOML ability adjustment (for testing) Specify 0. For testing.

P55: 0 CCUT2 With guaranteed phase capacity (VCOMH only)
P55: 1 CCUT2 With no guaranteed phase capacity (VCOMH only)
P56: 0 BST2 Normal
P56: 1 BST2 Ability UP
P57: 0 LPOW2 Normal
P57: 1 LPOW2 Low power

Parameter 6 (P6): Regulator circuit ability control 3

VONREG and VOFREG ability adjustment (for testing) Set to 0. For testing.

P65: 0 CCUT1 With guaranteed phase capacity
P65: 1 CCUT1 With guaranteed phase capacity
P66: 0 BST1 Normal
P66: 1 BST1 Ability UP
P67: 0 LPOW1 Normal
P67: 1 LPOW1 Low power

Parameter 7 (P7): Sets the pre-buffer ability of each source output pin. Specify 100.

P72 to P70: P bias
P76 to P74: N bias

P72/P76	P71/P75	P70/P74	Pre-buffer current consumption ratio
0	0	0	3
0	0	1	2.5
0	1	0	2
0	1	1	1.5
1	0	0	1
1	0	1	0.75
1	1	0	0.5
1	1	1	0.25

Parameter 8 (P8): Gray scale amplifier control 1
Enables 10 gray scale amplifiers by combining with the parameter A.
Specify 1 for all.

P87	P86	P85	P84	P83	P82	P81	P80
VOP8	VOP7	VOP6	VOP5	VOP4	VOP3	VOP2	VOP1

Parameter 9 (P9): Gray scale amplifier control 2
Enables 10 gray scale amplifiers by combining with the parameter B.
Specify 1 for all.

P91	P90
VOPL	VOPH

Parameter A (PA): Gray scale amplifier output Hz control 1
Enables 10 gray scale amplifiers by combining with the parameter 8.
Specify 1 for all.

PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
VOP8	VOP7	VOP6	VOP5	VOP4	VOP3	VOP2	VOP1

Parameter B (PB): Gray scale amplifier output Hz control 2
Enables 10 gray scale amplifiers by combining with the parameter 9.
Specify 1 for all.

PB1	PB0
VOPL	VOPH

Parameter C (PC): Set gray scale amplifier ability
Sets the ability of the gray scale amplifier.
Specify 001.

PC2 to PC0: Auxiliary
PC6 to PC4: Main

PC2/PC6	PC1/PC5	PC0/PC4	Gray scale amplifier current consumption ratio
0	0	0	0.0 (Stop)
0	0	1	1
0	1	0	1
0	1	1	2
1	0	0	0.5
1	0	1	1.5
1	1	1	2.5

Parameter D (PD): Set bias circuit ability
Sets the bias ability given to the gray scale amplifier.
Please set it to follows. PD2 to PD0 : 100, PD6 to PD4: 100

PD2 to PD0 : for VREFN

PD2	PD1	PD0	Gray scale amplifier current consumption ratio
0	0	0	0.0 (Stop)
0	0	1	4
0	1	0	2
0	1	1	1.33
1	0	0	1
1	0	1	0.8
1	1	0	0.67
1	1	1	0.57

PD6 to PD4 : for VREFP

PD6	PD5	PD4	Gray scale amplifier current consumption ratio
0	0	0	0.0 (Stop)
0	0	1	4
0	1	0	2
0	1	1	1.33
1	0	0	1
1	0	1	0.8
1	1	0	0.67
1	1	1	0.57

(22) Set Partial Power Control (Command code: 23h, Parameter: 7 bytes)
Power supply setup of the non-display area at the time of partial display is performed. P1 to P5 can set the state of the power supply circuit of the period for which non-display area is not refreshed etc. P6 and P7 can set the state of the power supply circuit of the refreshment period of non-display area etc.

D17	D16	D15	D14	D13	D12	D11	D10	Function
0	0	1	0	0	0	1	1	Command Partial Power control
*	*	*	P14	*	P12	P11	P10	Parameter 1 (P2) Sets VCOM ability
*	P26	P25	P24	*	P22	P21	P20	Parameter 2 (P2) Sets the boosting cycle
*	*	*	P34	P33	P32	P31	P30	Parameter 3 (P3) Regulator circuit control 1
P47	P46	P45	*	P43	P42	P41	P40	Parameter 4 (P4) Regulator circuit control 2
P57	P56	P55	*	*	*	*	*	Parameter 5 (P5) Regulator circuit control 3
*	P66	P65	P64	*	P62	P61	P60	Parameter 6 (P6) Set gray scale amplifier ability
*	P76	P75	P74	*	P72	P71	P70	Parameter 7 (P7) Sets bias circuit ability.

Parameter 1 (P1): Sets the recovery time and partial mode.

P12 to P10: Specifies the time at which power control returns, i.e., how many hours before driving the display line.

000: 0H
001: 1H
010: 2H
•
111: 7H

P14: Sets whether or not to boost VCOMH and VCOML in the non-display area similarly to P53 (boosting of VCOMH and VCOML) of Set Display Timing.

0: Not boost
1: Boost

Parameter 2 (P2): Sets frequency of the boosting clock of the 1st - 4th booster in the non-display area.

P22 to P20: Sets frequency of the boosting clock of the 1st and 2nd boosters in the non-display area.
P26 to P24: Sets frequency of the boosting clock of the 3rd and 4th boosters in the non-display area.

Determine while checking the display.

P22/P26	P21/P25	P20/P24	Frequency
0	0	0	= Stop
0	0	1	= Frequency in 1H × 8
0	1	0	= Frequency in 1H × 4
0	1	1	= Frequency in 1H × 2
1	0	0	= Frequency in 1H × 1
1	0	1	= Frequency in 1H / 2
1	1	0	= Frequency in 1H / 4
1	1	1	= Frequency in 1H / 8

Parameter 3 (P3) to Parameter 7 (P7): Sets power control of non-display area.
Discharge is not carried out even if it is set to OFF.

Parameter 3 (P3): See P4 of power control. However, VREG of P47 and P46 cannot be selected.

Parameter 4 (P4): See P5 of power control. However, VCOMH built-in resistor On of P54 cannot be selected.
When P40(VCOMH) P42(VCOML) P43 (VCOM) is set to 1, also in a non-displaying area, the same VCOM signal as a display area is generated.
A non-displaying area is set to Hi-Z when P43 (VCOM) is set to 0.

Parameter 5 (P5): See P6 of power control.

Parameter 6 (P6): See PC of power control.

Parameter 7 (P7): See PD of power control.

(23) Sleep In (Command code: 95h, Parameter: none)
Automatic command that executes multiple commands. Turns the display off, discharges power supply after displaying white, stops oscillation and puts into sleep state. After receiving the command, execution takes place immediately.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	0	1	0	1	0	1	Command: Sleep In command

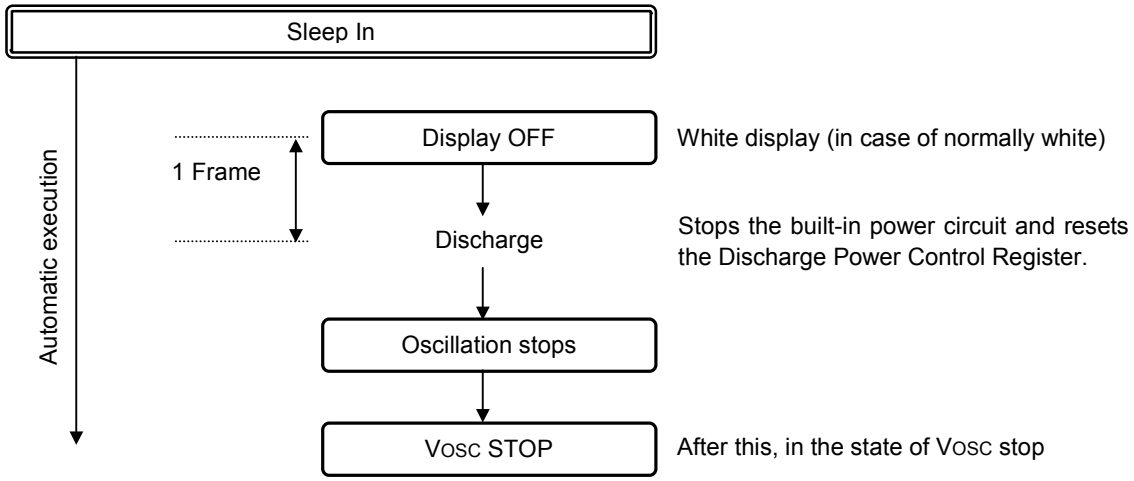
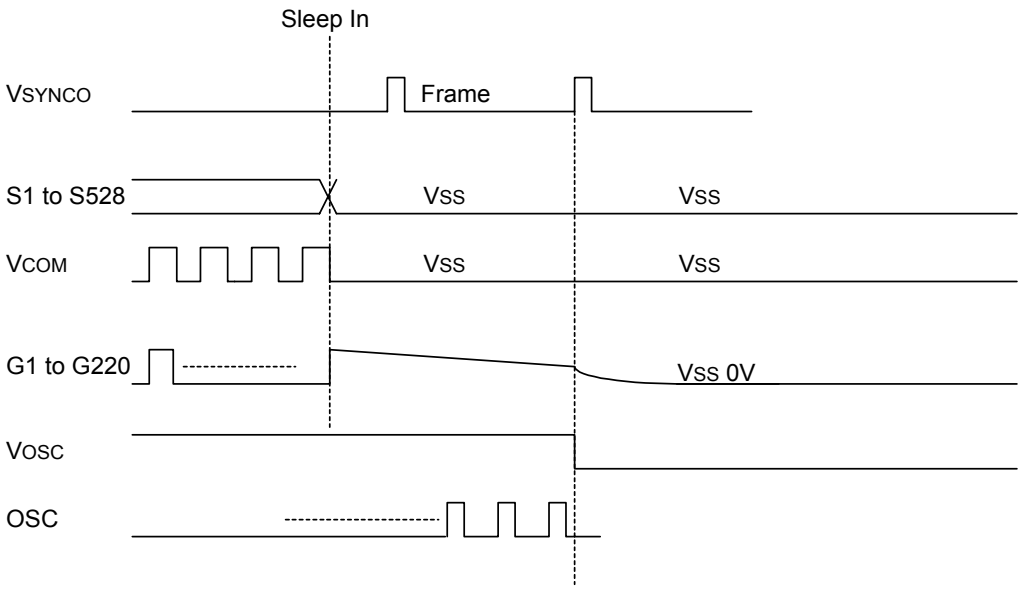


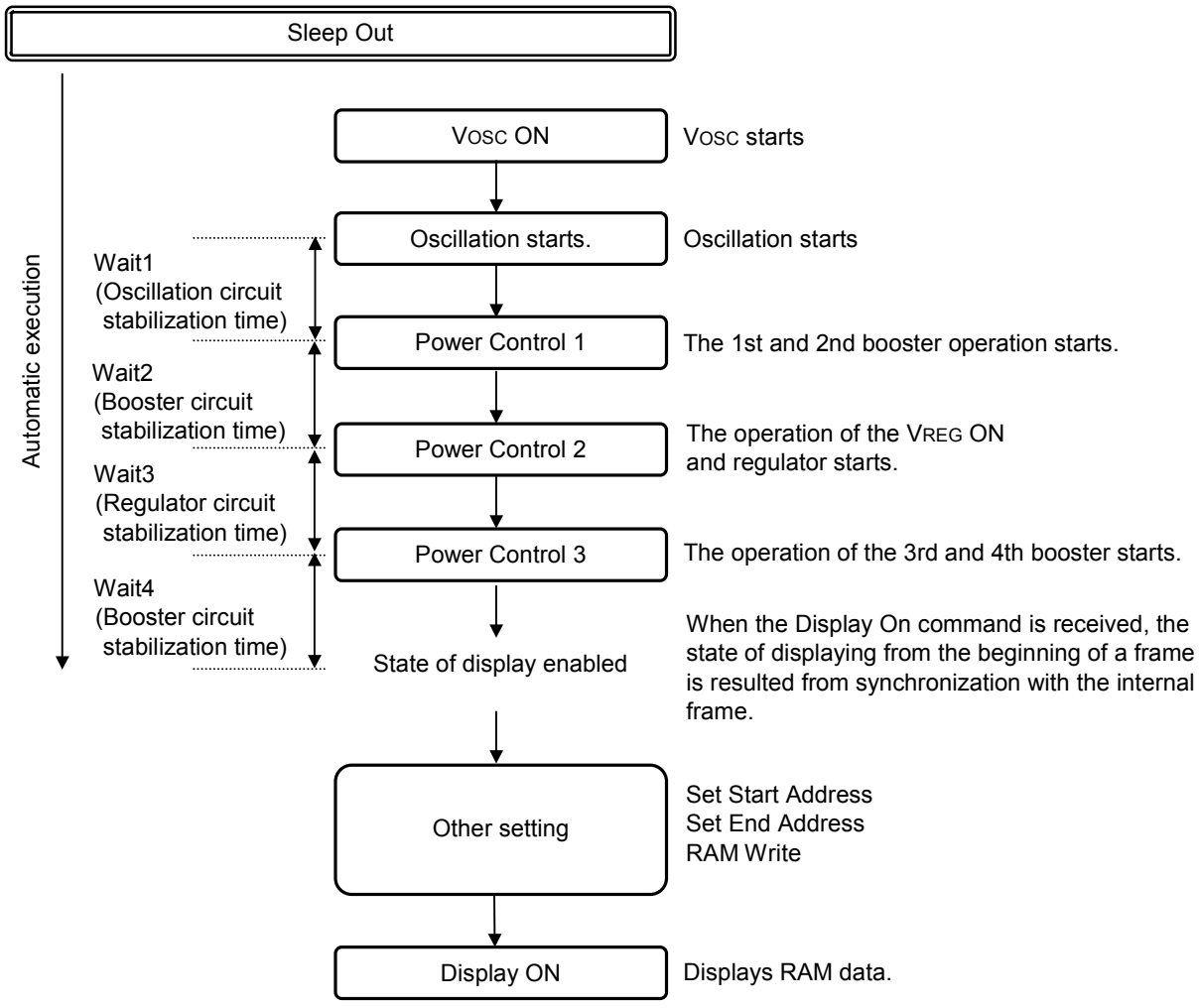
Fig.47 Sleep In Time Chart



In VSYNC interface, RGB transfer 2 and RGB transfer 3, no Sleep In takes place with no external clock entered. Be sure to enter the external clock. Change the MPU interface mode to cause Sleep In.

(24) Sleep Out (Command code: 94h, Parameter: none)
Automatic command that executes multiple commands. Starts VOSC and sequentially executes the Start Oscillation and Power Control command. When the Display ON command is received following startup of the built-in power supply. Displays starts from the beginning of the frame. If the Display ON command is received before the built-in power supply starts, wait is set automatically and the frame is displayed from the beginning after the built-in power supply is started. The boosting clock at the time of boost starting starts by 33h irrespective of the setting value (P4) of the display set. Before Wait4 end, it changes into the setting value of a display set automatically.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	0	1	0	1	0	0	Command: Sleep Out command



Once the Display ON command is issued, the display appears.
However, if the Display ON command is issued during the startup, the display appears after the startup of the power supply (following the state of display enabled). If the Display On command is not issued, the state of display enabled continues.

In VSYNC interface, RGB transfer 2 and RGB transfer 3, Sleep Out does not take place with no external clock entered. To execute Sleep Out, it is recommended to start in MPU interface mode and switch to other mode after Wait4.

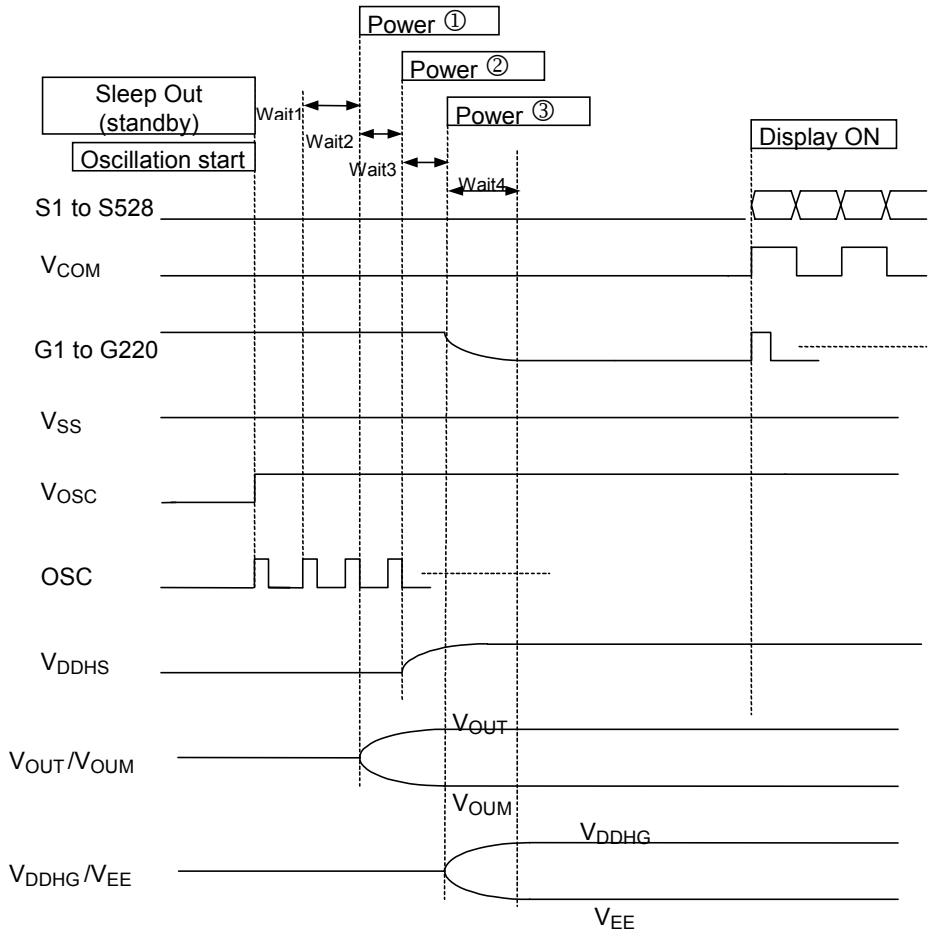


Fig.48 Sleep Out Time Chart

(25) VOSC OFF (Command code: 97h, Parameter: none)
Stop VCORE regulator, VOSC and VREG1 to VREG3. To set standby with the IC powered, enter this command to place in the state of low consumption. To change from the state of low consumption to the state of normal operation, enter the VOSC On command.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	0	1	0	1	1	1	Command: VOSC OFF command

TEST3,4=HIGH, LOW: VCORE is normally OFF(VCORE is outside input)
Constantly VCORE is OFF then it does not do the control of VCORE. It does only the halt of VOSC and VREG1 to VREG3.

TEST3,4=LOW, LOW: VCORE automatic control(VCORE is inside generation)
It does the halt of VCORE, VOSC and VREG1 to VREG3.

TEST3,4=LOW, HIGH: VCORE is normally ON (VCORE is inside generation)
Constantly VCORE is ON then it does not do the control of VCORE. It does only the halt of VOSC and VREG1 to VREG3.

(26) VOSC ON (Command code: 96h, Parameter: none)
Set VCORE to the state of normal operation and start VOSC and VREG1 to VREG3. Other commands cannot be entered for 10ms after entering the command.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	0	1	0	1	1	0	Command: VOSC ON command

TEST3,4=HIGH, LOW: VCORE is normally OFF(VCORE is outside input)
Constantly VCORE is OFF then it does not do the control of VCORE. It does only the halt of VOSC and VREG1 to VREG3.

TEST3,4=LOW, LOW: VCORE automatic control(VCORE is inside generation)
VOSC and VREG1 to VREG3 are ON in the command input when VCORE stop. In case of VCORE is operating, it does only VOSC ON.

TEST3,4=LOW, HIGH: VCORE is normally ON (VCORE is inside generation)
Constantly VCORE is ON then it does not do the control of VCORE. It does only the halt of VOSC and VREG1 to VREG3.

(27) Stop Oscillation (Command code: 93h, Parameter: none)
Stops oscillation of the built-in oscillation circuit.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	0	1	0	0	1	1	Command : Stop Oscillation

(28) Start Oscillation (Command code: 92h, Parameter: none)
Starts oscillation of the built-in oscillation circuit.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	0	1	0	0	1	0	Command : Start Oscillation

(29) Test (Command code: FFh, Parameter: 7 bytes)
Sets the function test mode. This is used for testing at shipping. The customer cannot use this command.
P1 to P3 are enabled when the TEST 1 pin is set to HIGH.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	1	1	1	1	1	1	1	Command Test
*	*	P15	P14	P13	P12	P11	P10	Parameter 1 (P1) For VREG adjustment (TEST 1)
*	*	*	*	P23	P22	P21	P20	Parameter 1 (P2) Constant current adjustment (TEST 1)
*	*	*	P34	P33	P32	P31	P30	Parameter 3 (P3) Oscillation frequency adjustment (TEST 1)
*	P46	P45	P44	P43	P42	P41	P40	Parameter 4 (P4) Discharge control 1
P57	P56	P55	P54	P53	P52	P51	P50	Parameter 5 (P5) Discharge control 2
*	*	P65	P64	P63	P62	P61	P60	Parameter 6 (P6) Gate driver test
P77	*	*	*	P73	P72	P71	P70	Parameter 7 (P7) Detector test

Parameter 1 (P1): For VREG adjustment (When TEST 1 pin = LOW, this is disabled.)

Parameter 2 (P2): For internal constant current adjustment (When TEST 1 pin = LOW, this is disabled.)

Parameter 3 (P3): For oscillation frequency adjustment (When TEST 1 pin = LOW, this is disabled.)

Parameter 4 (P4): Individual control of discharge function
0: Discharge
1: No discharge

P40: VLDO
P41: 1st and 2nd boosters
P42: 3rd booster
P43: 4th booster
P44: VOSC
P45: VCORE
P46: VREG

Parameter 5 (P5): Individual control of discharge function
0: Discharge
1: No discharge
P50: VDDHS
P51: VOFREG
P52: VONREG
P53: VDDRH
P54: VDDRL
P55: VCOMH
P56: VCOM
P57: VCOML

Parameter 6 (P6) Test function of gate driver (The customer cannot use this pin.)
P60: All-pin HIGH 0: Normal operation 1: All-pin VDDHG (with time difference)
P61: Test 1 0: Normal operation 1: 1, 5, 9 …pin VDDHG
P62: Test 2 0: Normal operation 1: 2, 6, 10 …pin VDDHG
P63: Test 3 0: Normal operation 1: 3, 7, 11 …pin VDDHG
P64: Test 4 0: Normal operation 1: 4, 8, 12 …pin VDDHG
P65: Reverse 0: Normal operation 1: Full-output logic reverse

Parameter 7 (P7): Test function of detector and VSYNC synchronization cancellation function (The customer cannot use this pin.)
P70: VDD2-series detector power saving
0: OFF 1: Normal operation

P71: V_{DD2}-series detector power saving
0: Power-up 1: Normal operation

P72: V_{DD2}-series detector power saving
0: OFF 1: Normal operation

P73: V_{DDI}-series detector power-up
0: Power-up 1: Normal operation

P77: Cancels the function execution in synchronization with VSYNC of all commands.
0: Synchronized with VSYNC 1: Exectes immediately.

(30) NOP (Command code: 00h, Parameter: 0 byte)
This is a non-operation command. This command does not affect the system operation at all.

D17	D16	D15	D14	D13	D12	D11	D10	Function
0	0	0	0	0	0	0	0	Command: Non Operation command

(31) Status Read (Command code: E8h, Parameter: 3 bytes)
The internal state of the IC can be read.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	1	1	0	1	0	0	0	Command: Status Read
P17	P16	P15	P14	P13	P12	P11	P10	Status 1 (P1)
P27	P26	P25	P24	P23	P22	P21	P20	Status 2 (P2)
*	P36	P35	P34	P33	P32	P31	P30	Status 3 (P3)

Parameter 1 (P1):
P10: 1: Turns the display ON.
0: Turns the display OFF.

P11: 1: Sleep Out
0: Sleep In

P12: 1: Partial In
0: Partial Out

P13: 1: High-speed RAM write mode
0: Normal RAM Write

P14: 1: 8-color display mode
0: 262k-color display mode

P15: 1: Scans in row direction.
0: Scans in column direction.

P16: Area scroll mode P40

P17: Area scroll mode P41

Parameter 2 (P2):
P20 to 27: RAM line address

Parameter 3 (P3):

P30: 1: Source ON
0: Source OFF
P31: 1: Pre-buffer drive.
0: DAC drive:
P32: 1: VCOM boost ON
0: VCOM boost OFF
P33: Wait 1
P34: Wait 2
P35: Wait 3
P36: Wait 4

(32) Revision Read (Command code: E9, Parameter: none)
The command code is valid only at the serial interface mode.
Revision of the IC can be read. For the parallel interface, revision can be read by setting A0 to LOW and $\overline{RD}$ to LOW without setting the command code.

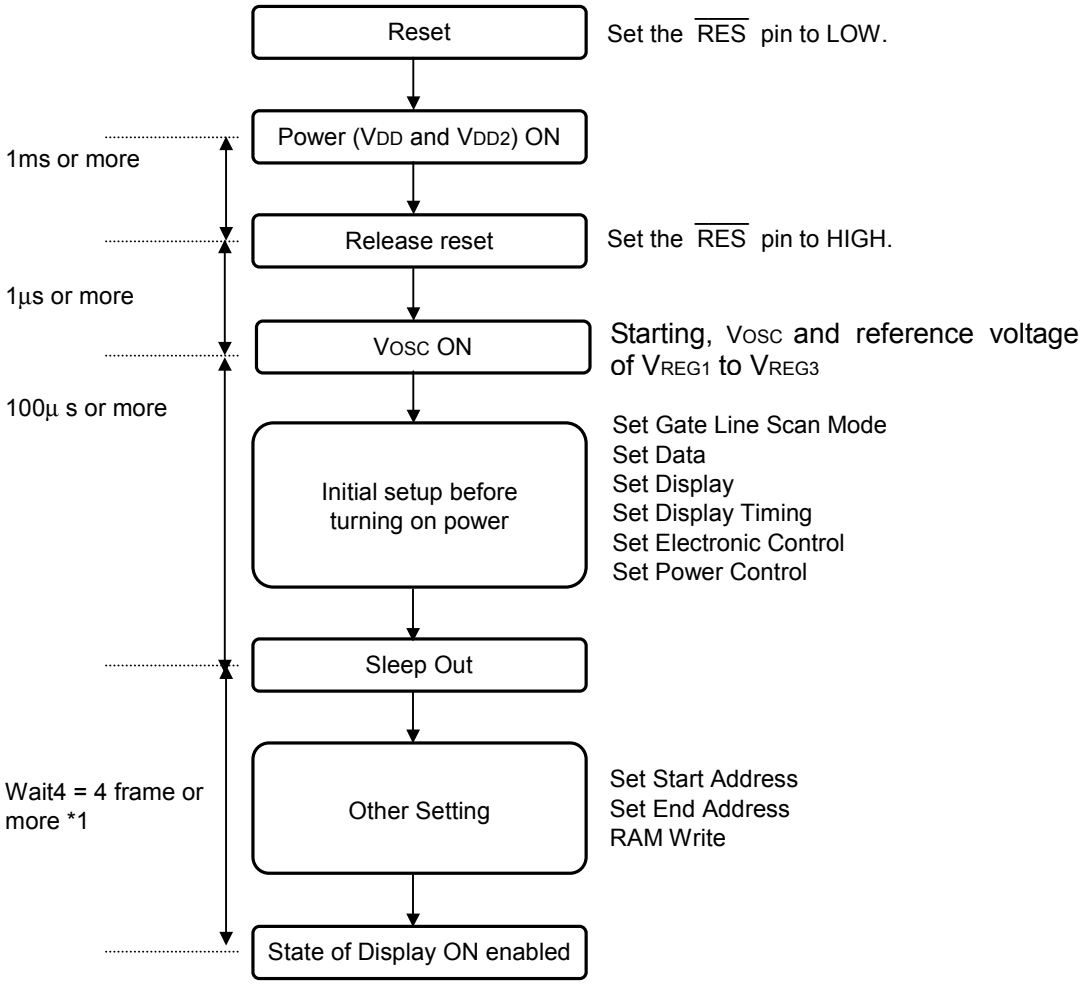
D17	D16	D15	D14	D13	D12	D11	D10	Function
1	1	1	0	1	0	0	1	Command: Revision Read

(33) Soft Reset (Command code: 99, Parameter: none)
The same reset as hard reset can be used with this command without hard resetting.

D17	D16	D15	D14	D13	D12	D11	D10	Function
1	0	0	1	1	0	0	1	Command : Soft Reset

7.5 Instruction Setup Example (Reference)

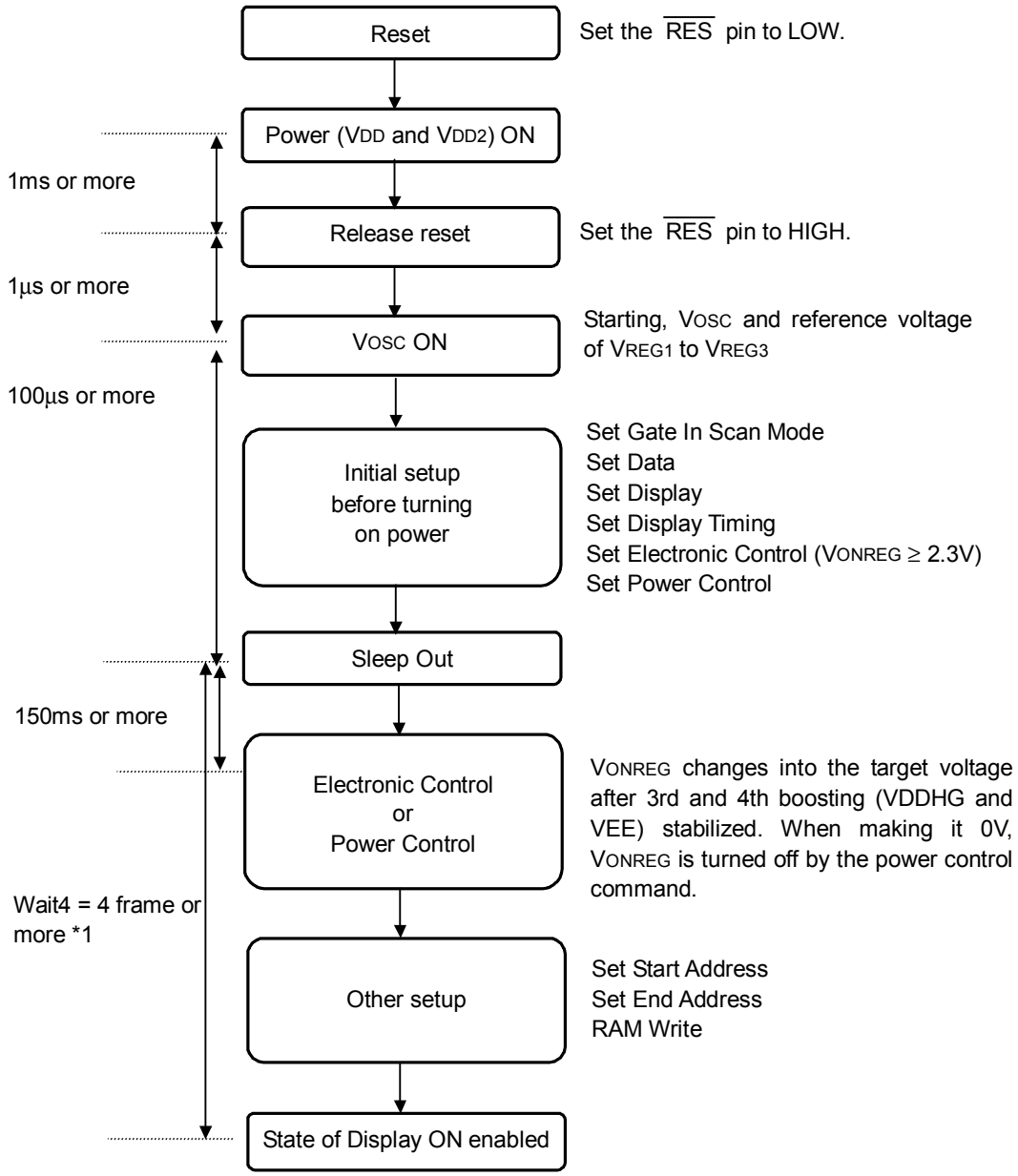
7.5.1 Initial Setup to Display-ON (V_{CORE} forceful ON, V_{CORE} forceful OFF, VDC4 is 2.3V or more)



After the state of Display ON enabled, display is enabled at any time. If the Display ON command is received before the state of display enabled, wait takes place automatically until the state of Display ON enabled is reached.

*1: Wait 4 is for reference. This value depends on the LCD panel lode, it should be decided after evaluation.

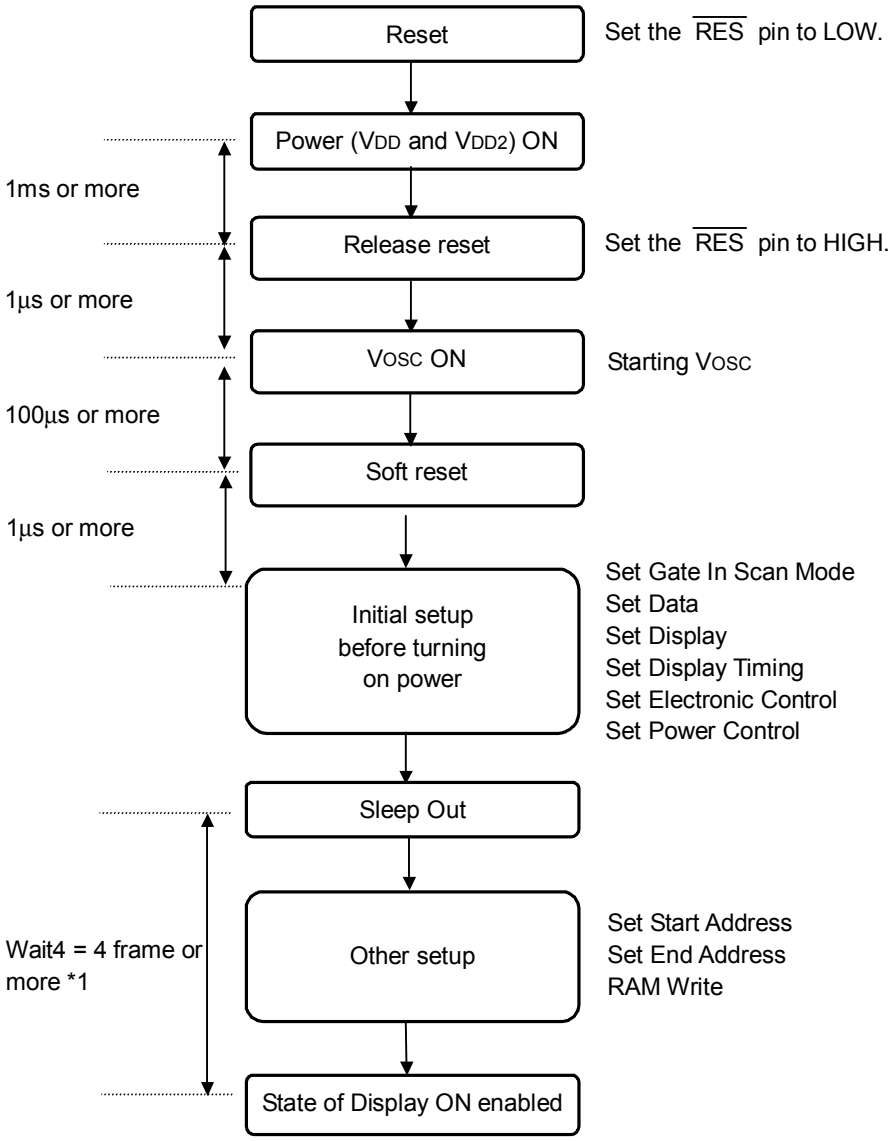
7.5.2 Initial Setup to Display-ON (V_{CORE} forceful ON, V_{CORE} forceful OFF, VDC4 is less than 2.3V, V_{ONREG} is used)



It can display at any time after which can be display turned on state. It is necessary for the state which can be display turned on to have set V_{CONREG} as the target voltage by the electronic volume or power control command. The display ON command should perform after changing into the target voltage of V_{CONREG}. However, when the time of a display ON command being executed is during the automatic wait period after sleep out, it waits automatically until a wait period expires.

*1: Wait 4 is for reference. This value depends on the LCD panel lode, it should be decided after evaluation.

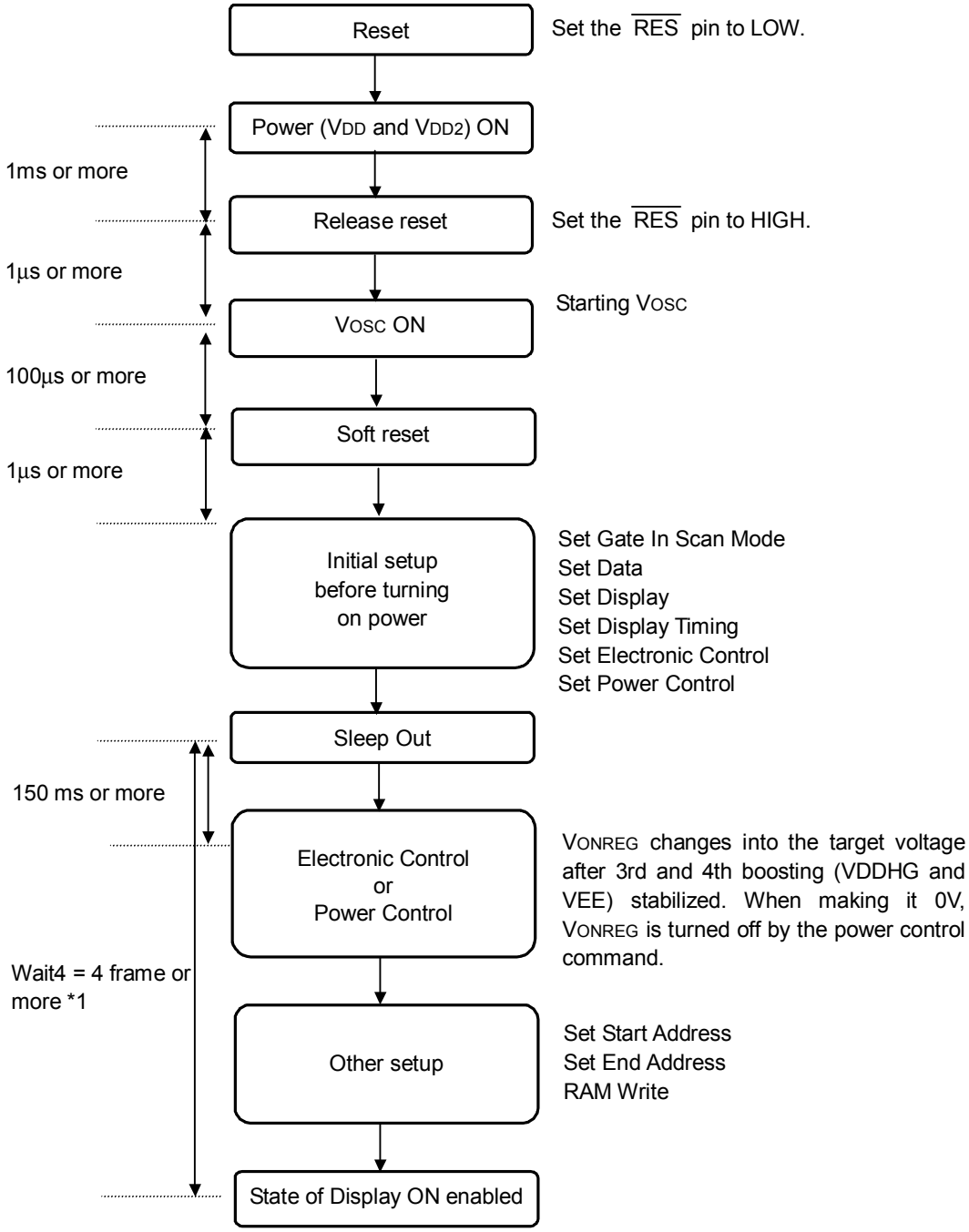
7.5.3 Initial Setup to Display-ON (Normal use of V_{CORE}, VDC4 is 2.3V or more)



After the state of Display ON enabled, display is enabled at any time. If the Display ON command is received before the state of display enabled, wait takes place automatically until the state of Display ON enabled is reached.

*1: Wait 4 is for reference. This value depends on the LCD panel lode, it should be decided after evaluation.

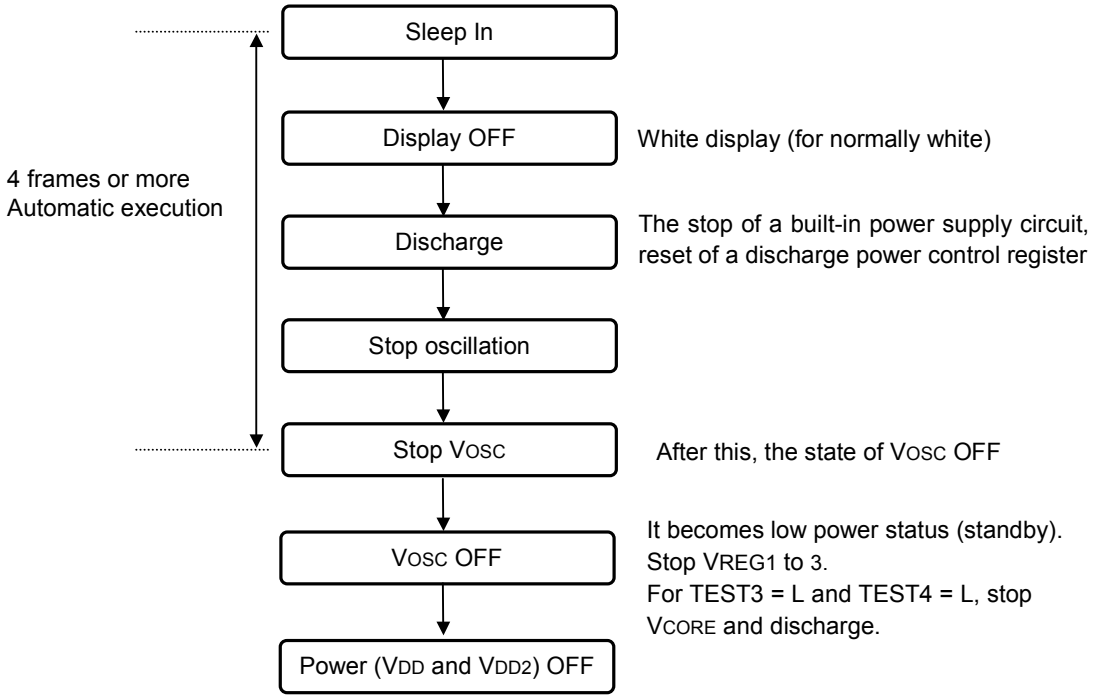
7.5.4 Initial Setup to Display-ON (Normal use of VCORE, VDC4 is less than 2.3V and VONREG is used)



It can display at any time after which can be display turned on state. It is necessary for the state which can be display turned on to have set VCONREG as the target voltage by the electronic volume or power control command. The display ON command should perform after changing into the target voltage of VCONREG. However, when the time of a display ON command being executed is during the automatic wait period after sleep out, it waits automatically until a wait period expires.

*1: Wait 4 is for reference. This value depends on the LCD panel lode, it should be decided after evaluation.

7.5.5 Power OFF Sequence



Note: To turn ON power again, perform the power ON sequence from reset.

8. ABSOLUTE MAXIMUM RATINGS

Table 33 Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DDI}	-0.3 to +4.6	V
Supply voltage (2)	V_{CORE}	-0.3 to +3.3	
Supply voltage (3)	V_{DD2}	-0.3 to +4.6	
Supply voltage (4)	V_{DD}	-0.3 to +4.6	
Supply voltage (5)	V_{OUT}	-0.3 to +7.0	
Supply voltage (6)	V_{OUTM}	-7.0 to +0.3	
Supply voltage (7)	V_{DDHS}	-0.3 to +7.0	
Supply voltage (8)	V_{DDRH}	-0.3 to +7.0	
Supply voltage (9)	V_{DDRL}	-0.3 to +7.0	
Supply voltage (10)	V_{DDHG}	-0.3 to +18.0	
Supply voltage (11)	V_{EE}	-18.0 to +0.3	
Supply voltage (12)	V_{ONREG}	-0.3 to +7.0	
Supply voltage (13)	V_{OFREG}	-0.3 to +7.0	
Supply voltage (14)	V_{COMH}	-0.3 to +7.0	
Supply voltage (15)	V_{COML}	-7.0 to +0.6	
Supply voltage (16)	V_{COMW}	-0.3 to +7.0	
Logic input voltage	V_{IN}	-0.3 to V_{DDI}+0.3	
Logic output voltage	V_{OUT}	-0.3 to V_{DDI}+0.3	
Operating temperature	T_{opr}	-40 to +85	°C
Storage temperature	T_{stg}	-55 to +125	

Notes:
1 Unless otherwise noted, all voltages are specified based on V_{SS}=0V.
2 If the IC exceeds its absolute maximum ratings, it may be damaged. Also, if the IC is operated with the absolute maximum ratings for a long time, its reliability may drop.
3 The power voltage (5) to (14) cannot be used by turning on the external power supply.
4 The absolute maximum rating of the potential difference between V_{DDHG} to V_{EE} is 33V.
5 The VDD2 absolute maximum ratings of 4.6V is standards when it uses it before 1st boosting or doesn't use the boosting power supply. As for the VDD2, 3.5V is maximum that is 1/2 of the VOUT absolute maximum ratings.

9. RECOMMENDED OPERATING CONDITIONS

Table 34 Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Operating voltage	Unit
Supply voltage (1)	V_{DDI}	1.65 to 3.3	V
Supply voltage (2)	V_{CORE}	2.3 to 3.1	
Supply voltage (3)	V_{DD}	2.3 to 3.1	
Supply voltage (4)	V_{DD2}	2.3 to 3.1	
Supply voltage (5)	V_{OUT}	4.6 to 6.2	
Supply voltage (6)	V_{OUTM}	-6.2 to 0	
Supply voltage (7)	V_{DDHS}	T.B.D. to 5.5	
Supply voltage (8)	V_{DDRH}	T.B.D. to 5.5	
Supply voltage (9)	V_{DDRL}	0.0 to 1.55	
Supply voltage (10)	V_{DDHG}	7.0 to 17.0	
Supply voltage (11)	V_{EE}	-15.0 to -5.0	
Supply voltage (12)	V_{ONREG}	2.9 to 5.5	
Supply voltage (13)	V_{OFREG}	0 to 5.1	
Supply voltage (14)	V_{COMH}	3.0 to 5.5	
Supply voltage (15)	V_{COML}	V_{OUTM} to 0.0	
Supply voltage (16)	V_{COMW}	1.5 to 3.05	

Notes:
1 The IC operations are guaranteed under the recommended operating conditions only.
2 To prevent noise, a bypass capacitor must be inserted into the line close to power pins.
3 These operations are not guaranteed if a quick voltage change occurs during IC operation.
4 The power voltage (5) to (14) cannot be used by turning on the external power supply.
5 The recommended operating rating of the potential difference between V_{DDHG} to V_{EE} is 30V.

10. DC CHARACTERISTICS

Table 35 DC Characteristics

V_{SS}=0V, V_{DDI}=1.65 to 3.3V, V_{CORE}=1.65 to 3.1V, T_a=-40 to +85°C

Parameter	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
LOW level input voltage	V_{IL}	—	V_{SS}	—	0.3×V_{DDI}	V	Logic-series input voltage
HIGH level input voltage	V_{IH}		0.7×V_{DDI}	—	V_{DDI}		
Input leak current (1)	I_{LI1}	V_{IN}=V_{DDI} or V_{SS}	-1.0	—	1.0	μA	Logic-series input voltage
Input capacity	C_{IN}	T_a=25°C, f=1MHz	—	—	25	pF	Logic-series input voltage
LOW level output voltage	V_{OL1}	V_{DD}=2.8V I_{OL}=0.06mA I_{OH}=-0.06mA	V_{SS}	—	V_{SS}+0.3	V	Logic series output voltage
HIGH level output voltage	V_{OH1}		V_{DDI}-0.3	—	V_{DDI}		
V_{REG} voltage	V_{REG}	V_{DD}=2.8V, T_a=25°C V_{DD2}=2.8V V_{OUT}=5.6V	3.45	3.5	3.55	V	V_{REG}
Output voltage deviation(DAC)	ΔVs	T_a=25°C	—	±10	±20	mV	S1 to S528
1st booster ability (Internal resistor) *1	R_{VOUT12}	V_{DD2}=2.8V V_{DC1}=V_{DD2}	—	190	240	Ω	V_{OUT}
2nd booster ability (Internal resistor) *1	R_{VOUT2}	V_{DD2}=2.8V V_{DC2}=V_{DD2}	—	220	275	Ω	V_{OUTM}
3rd booster ability (-double) (Internal resistor) *1	R_{VOUT3}	V_{DD2}=2.8V V_{OFREG}=5V V_{DC3}=V_{OFREG}	—	600	900	Ω	V_{EE}
4th booster ability (Internal resistor) *1	R_{VOUT4}	V_{DD2}=2.8V V_{OFREG}=5V V_{DC3}=V_{OFREG}	—	400	1500	Ω	V_{DDHG}
Static current consumption 1 *2	I_{DDIQ}	VDDI =VCORE= VDD =VDD2=2.8V	—	0.1	1.0	mA	V_{DDI}
	I_{COREQ}		—	1.0	2.0	mA	V_{CORE}
	I_{DDQ}		—	0.1	1.0	mA	V_{DD}
	I_{DD2Q}		—	0.1	1.0	mA	V_{DD2}
Dynamic current consumption 1 *3	I_{DDI1}	*5 VDDI =VCORE= VDD =VDD2=2.8V	—	0.1	1.0	μA	V_{DDI}
	I_{CORE1}		—	100	150	μA	V_{CORE}
	I_{DD1}		—	30	45	μA	V_{DD}
	I_{DD21}		—	1560	2400	μA	V_{DD2}
Dynamic current consumption 3 *4	I_{DDI2}	*6 VDDI =VCORE= VDD =VDD2=2.8V	—	30	45	μA	V_{DDI}
	I_{CORE2}		—	1000	1500	μA	V_{CORE}
	I_{DD2}		—	20	40	μA	V_{DD}
	I_{DD22}		—	85	130	μA	V_{DD2}

*1 T_a = 25°C, Capacitance = 1uF, Boosting frequency =1H x 1

*2 After resetting, current consumption in the state of initial value of the command. T_a=25°C
(For CMOS, fix the input level at V_{DDI} or V_{SS}, since current flows into the input circuit when the input level is at the intermediate voltage level.)

*3 Current consumption during still picture display (built-in power supply used, without access to RAM) T_a=25°C.

*4 Current consumption during access to RAM ($\overline{WR}$) (display is OFF) T_a=25°C.

*5 After resetting, commands other than Sleep Out, Power Control All ON, RAM Write and Display ON are initial values. RAM data is the state in which the following data is written alternately.
R(101010)G(101010)B(101010), R(010101)G(010101)B(010101)

*6 Current consumption when the following display data is continuously written to RAM alternately at the frequency of 2.5MHz.
R(101010)G(101010)B(101010), R(010101)G(010101)B(010101)

11. AC CHARACTERISTICS

11.1 Oscillation Frequency

The following defines the clock frequencies to enter the oscillation frequency of built-in oscillator and external clocks into OSC pin.

Table 36 Oscillation Frequency

V_{SS}=0V, V_{DDI}=1.65 to 3.3V, V_{CORE}=V_{DD}=V_{DD2}=2.3 to 3.1V, T_a=25°C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation frequency	f_{OSC}	When built-in oscillator circuit is used	950	1000	1050	kHz
External clock input frequency	f_{OSCI}	—	900	1000	1100	kHz

11.2 Parallel Interface

11.2.1 The 80-Series MPUs

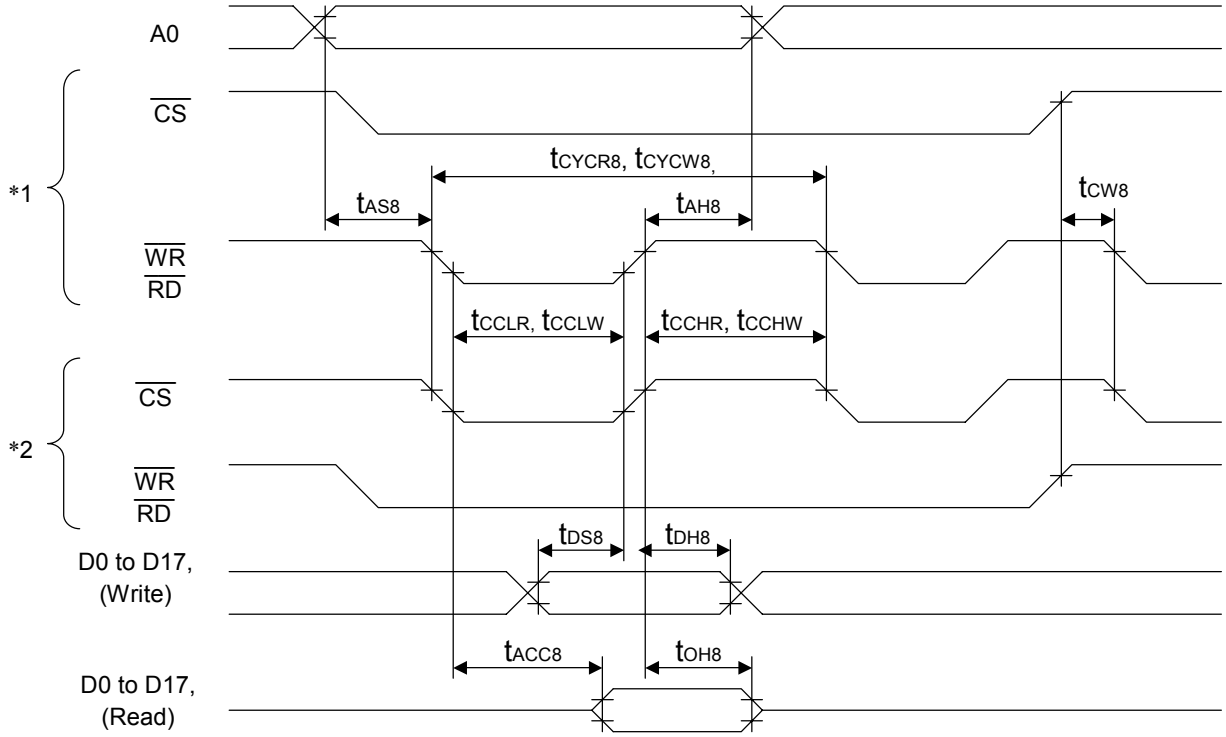


Fig.49 The 80-Series MPUs

*1 If $\overline{CS}$ = LOW and if accessed by $\overline{WR}$ or $\overline{RD}$ signal
*2 If $\overline{WR}$=LOW and if accessed by $\overline{CS}$ signal

11. AC CHARACTERISTICS

● Normal write mode

V_{SS}=0V, V_{DDI}=1.65 to 3.3V, V_{CORE}=2.7 to 3.1V, T_a=-40 to +85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
A0 hold time	t_{AH8}	—	10	—	ns
A0 setup time	t_{AS8}	—	10	—	
Write system cycle time	t_{CYCW8}	—	100	—	
$\overline{WR}$ LOW level pulse width	t_{CCLW}	—	40	—	
$\overline{WR}$ HIGH level pulse width	t_{CCHW}	—	30	—	
Read system cycle time	t_{CYCR8}	—	500	—	
$\overline{RD}$ LOW level pulse width	t_{CCLR}	—	350	—	
$\overline{RD}$ HIGH level pulse width	t_{CCHR}	—	50	—	
$\overline{CS}$-$\overline{WR}$ and $\overline{RD}$ time	t_{CW8}	—	20	—	
Data setup time	t_{DS8}	—	10	—	
Data hold time	t_{DH8}	—	10	—	
$\overline{RD}$ access time	t_{ACC8}	CL=50pF	—	300	
Output disable time	t_{OH8}		5	50	

● Normal write mode

V_{SS}=0V, V_{DDI}=V_{CORE}=1.65 to 2.7V, T_a=-40 to +85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
A0 hold time	t_{AH8}	—	20	—	ns
A0 setup time	t_{AS8}	—	20	—	
Write system cycle time	t_{CYCW8}	—	200	—	
$\overline{WR}$ LOW level pulse width	t_{CCLW}	—	80	—	
$\overline{WR}$ HIGH level pulse width	t_{CCHW}	—	60	—	
Read system cycle time	t_{CYCR8}	—	500	—	
$\overline{RD}$ LOW level pulse width	t_{CCLR}	—	350	—	
$\overline{RD}$ HIGH level pulse width	t_{CCHR}	—	50	—	
$\overline{CS}$-$\overline{WR}$ and $\overline{RD}$ time	t_{CW8}	—	30	—	
Data setup time	t_{DS8}	—	20	—	
Data hold time	t_{DH8}	—	20	—	
$\overline{RD}$ access time	t_{ACC8}	CL=50pF	—	300	
Output disable time	t_{OH8}		10	100	

*3 All timings are specified based on the 20% and 80% of V_{DDI}.

*4 The rise and fall times (t_r and t_f) of the input signal are specified for less than 10ns. If high-speed system cycle time is used, $t_r + t_f \leq t_{CYCW8} - t_{CCLW} - t_{CCHW}$ or $t_r + t_f \leq t_{CYCR8} - t_{CCLR} - t_{CCHR}$ must be satisfied.

*5 t_{CCLW} and t_{CCLR} are specified for the overlap period when $\overline{CS}$ is at LOW level and $\overline{WR}$ and $\overline{RD}$ are at LOW level.

11.2.2 The 68-Series MPUs

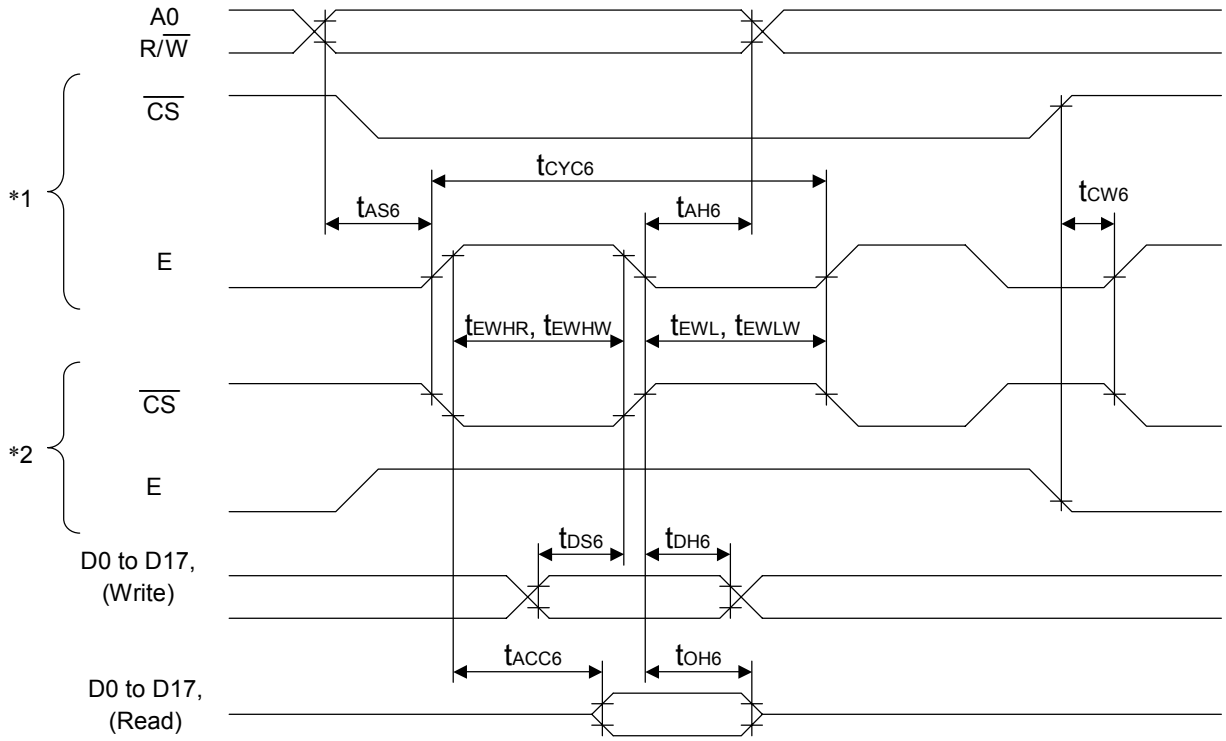


Fig.50 The 68-Series MPUs

*1 If $\overline{CS}$ = LOW and if accessed by E signal
*2 If E = HIGH and if accessed by $\overline{CS}$ signal

11. AC CHARACTERISTICS

● Normal write mode

V_{SS}=0V, V_{DDI}=1.65 to 3.3V, V_{CORE}=2.7 to 3.1V, T_a=-40 to +85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
A0 hold time	t_{AH6}	—	10	—	ns
A0 setup time	t_{AS6}	—	10	—	
Write system cycle time	t_{CYCW6}	—	100	—	
E (Write) HIGH level pulse width	t_{EWHW}	—	40	—	
E (Write) LOW level pulse width	t_{EWLW}	—	30	—	
Read system cycle time	t_{CYCR6}	—	500	—	
E (Read) HIGH level pulse width	t_{EWHR}	—	350	—	
E (Read) LOW level pulse width	t_{EWLR}	—	50	—	
$\overline{CS}$-E time	t_{CW6}	—	20	—	
Data setup time	t_{DS6}	—	10	—	
Data hold time	t_{DH6}	—	10	—	
Read access time	t_{ACC6}	CL=50pF	—	300	
Output disable time	t_{OH6}		10	50	

● Normal write mode

V_{SS}=0V, V_{DDI}=V_{CORE}=1.65 to 2.7V, T_a=-40 to +85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
A0 hold time	t_{AH6}	—	20	—	ns
A0 setup time	t_{AS6}	—	20	—	
Write system cycle time	t_{CYCW6}	—	200	—	
E (Write) HIGH level pulse width	t_{EWHW}	—	80	—	
E (Write) LOW level pulse width	t_{EWLW}	—	60	—	
Read system cycle time	t_{CYCR6}	—	500	—	
E (Read) HIGH level pulse width	t_{EWHR}	—	350	—	
E (Read) LOW level pulse width	t_{EWLR}	—	50	—	
$\overline{CS}$-E time	t_{CW6}	—	30	—	
Data setup time	t_{DS6}	—	20	—	
Data hold time	t_{DH6}	—	20	—	
Read access time	t_{ACC6}	CL=50pF	—	300	
Output disable time	t_{OH6}		10	100	

*3 All timings are specified based on the 20% and 80% of V_{DDI}.

*4 The rise and fall times (t_r and t_f) of the input signal are specified for less than 10ns.
If high-speed system cycle time is used, $t_r + t_f \leq t_{CYC6} - t_{EWLW} - t_{EWHW}$ or $t_r + t_f \leq t_{CYC6} - t_{EWLR} - t_{EWHR}$ must be satisfied.

*5 t_{EWLW} and t_{EWLR} are specified for the overlap period when $\overline{CS}$ is at LOW level and E is at HIGH level.

11.3 Serial Interface

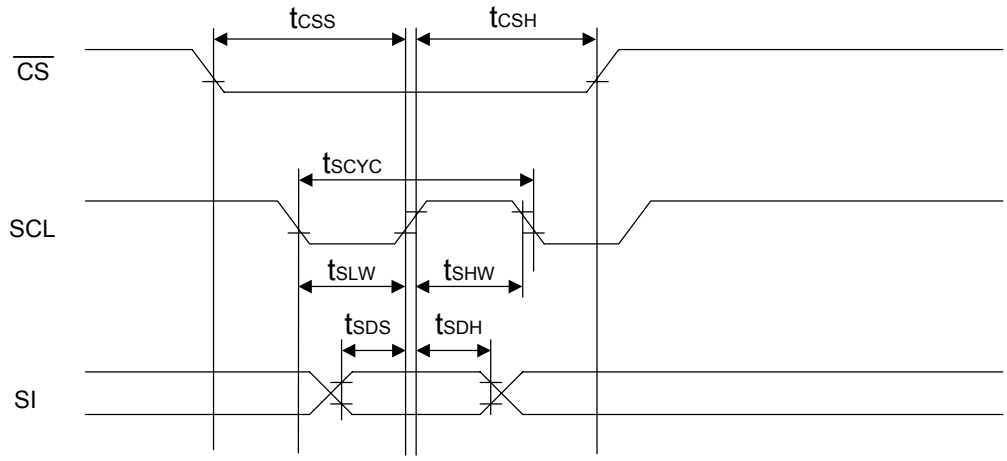


Fig.51 Serial Interface

V_{SS}=0V, V_{DDI}=1.65 to 3.3V, V_{CORE}=2.7 to 3.1V, T_a=-40 to +85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
SCL cycle	t_{SCYC}	—	50	—	ns
SCL LOW level pulse width	t_{SLW}	—	10	—	
SCL HIGH level pulse width	t_{SHW}	—	10	—	
Data setup time	t_{SDS}	—	10	—	
Data hold time	t_{SDH}	—	10	—	
$\overline{CS}$ setup time	t_{CSS}	—	20	—	
$\overline{CS}$ hold time	t_{CSH}	—	30	—	

V_{SS}=0V, V_{DDI}=V_{DD}=1.65 to 2.7V, T_a=-40 to +85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
SCL cycle	t_{SCYC}	—	100	—	ns
SCL LOW level pulse width	t_{SLW}	—	20	—	
SCL HIGH level pulse width	t_{SHW}	—	20	—	
Data setup time	t_{SDS}	—	20	—	
Data hold time	t_{SDH}	—	20	—	
$\overline{CS}$ setup time	t_{CSS}	—	30	—	
$\overline{CS}$ hold time	t_{CSH}	—	45	—	

*1 All timings are specified based on the 20% and 80% of V_{DDI}.
*2 The rise and fall times (t_r and t_f) of the input signal are specified for less than 10ns.

11.4 Resetting

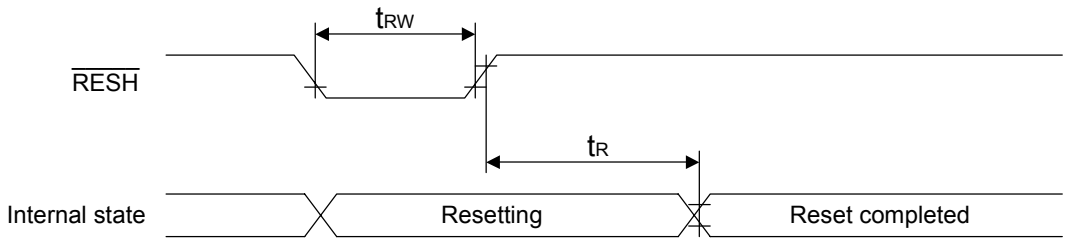


Fig.52 Resetting

V_{SS}=0V, V_{DDI}=V_{CORE}=1.65 to 3.1V, T_a=-40 to +85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Reset time	t_R	—	—	1	µs
Reset LOW level pulse width	t_{RW}	—	1	—	

*1 All timings are specified based on the 20% and 80% of V_{DDI}.
*2 We recommend to hold the $\overline{RES}$ pin to LOW during power-on conditions.
*3 Applied when resetting while the power supply is stabilized.

11.5 Source Output

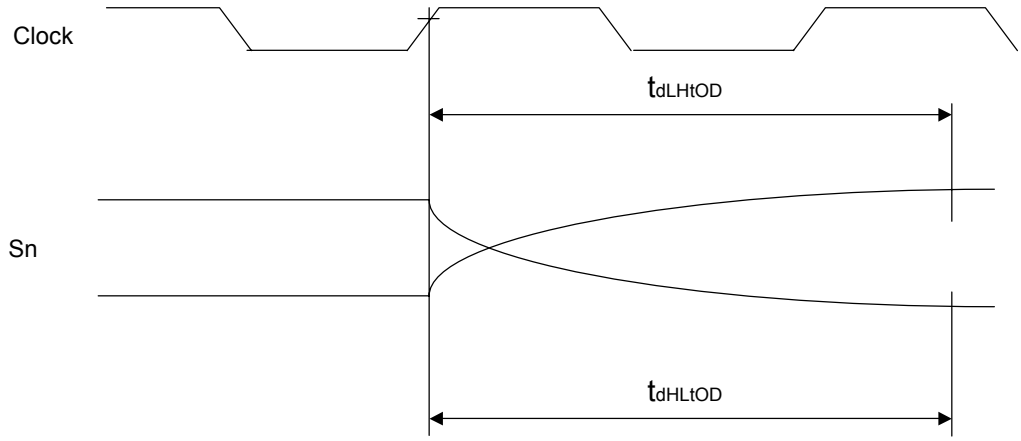


Fig.53 Source Output

V_{SS}=0V, V_{DDHS}=4.5V, T_a=-40 to +85°C

Parameter	Symbol	Condition	Typ.	Max.	Unit
Clock Sn output delay time (LOW→HIGH)	t_{dLHtOD}	CL=20pF, RL=1.1KΩ	—	30	µs
Clock Sn output delay time (HIGH→LOW)	t_{dHLtOD}	CL=20pF, RL=1.1KΩ	—	30	

*1 Specified based on the clock rise edge defined by the Set Display Timing command at P1.
*2 Sn can be S1 to S528 outputs.
*3 Clock Sn output delay time-2 is set to ±50mV.

11.6 RGB Interface

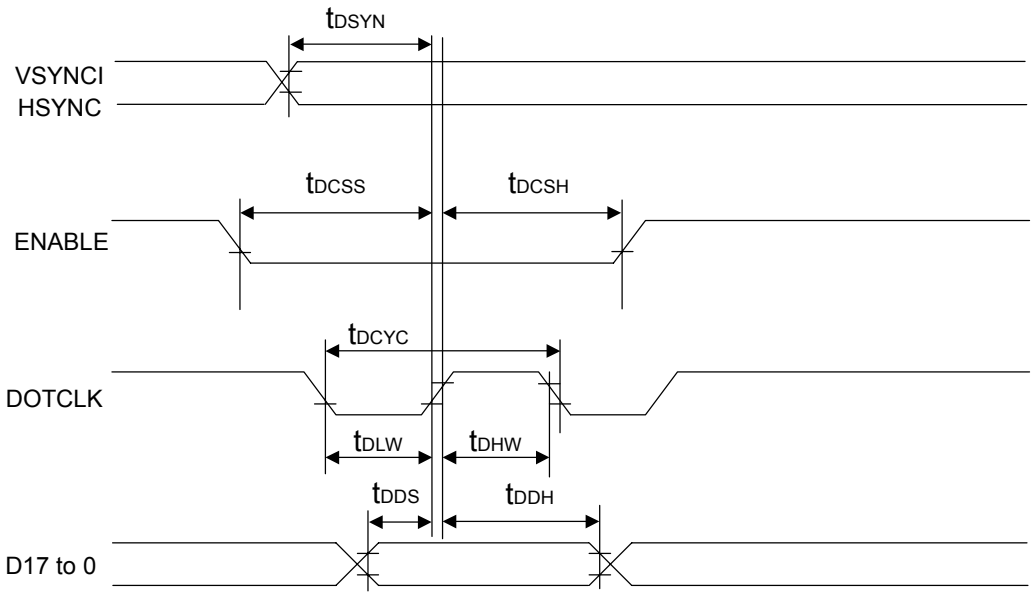


Fig.54 RGB Interface

VSS=0V, VDDI=1.65 to 3.3V, VCORE=2.7 to 3.1V, Ta=-40 to +85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
DOTCLK cycle	t_{DCYC}	—	100	—	ns
DOTCLK LOW level pulse width	t_{DLW}	—	30	—	
DOTCLK HIGH level pulse width	t_{DHW}	—	30	—	
Data setup time	t_{DDS}	—	10	—	
Data hold time	t_{DDH}	—	20	—	
ENABLE setup time	t_{DCSS}	—	75	—	
ENABLE hold time	t_{DCSH}	—	75	—	
VSYNC setup time	t_{DSYV}	—	10	—	
HSYNC setup time	t_{DSYH}	—	10	—	

VSS=0V, VDDI=VCORE=1.65 to 2.7V, Ta=-40 to +85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
DOTCLK cycle	t_{DCYC}	—	200	—	ns
DOTCLK LOW level pulse width	t_{DLW}	—	60	—	
DOTCLK HIGH level pulse width	t_{DHW}	—	60	—	
Data setup time	t_{DDS}	—	20	—	
Data hold time	t_{DDH}	—	40	—	
ENABLE setup time	t_{DCSS}	—	150	—	
ENABLE hold time	t_{DCSH}	—	150	—	
VSYNC setup time	t_{DSYV}	—	20	—	
HSYNC setup time	t_{DSYH}	—	20	—	

*1 All timings are specified based on the 20% and 80% of VDDI.
*2 The rise and fall times (t_r and t_f) of the input signal are specified for less than 10ns.

12. NOTES

When using these development specifications, note the following points.
1. The contents of these development specifications are subject to change without notice for improvement.
2. There is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party.

Examples shown in these development specifications are for understanding our products, and we are not responsible for any circuit problems that may occur when using them.

When using the S1D19105 series, note the following points:

IC handling notes against the light:
As a semiconductor chip is principally identical to a solar cell, its performance may change if exposed to bright light. Therefore, the IC may malfunction if exposed to light.
① Design and mount the IC so that it is not exposed to light during actual operation.
② In the test process, check the design and mounting of the IC so that it is not exposed to light.
③ Take all surfaces, top, bottom and sides, of the IC chip into consideration when blocking out light.

IC handling notes on ambient noise and others:
① Though the S1D19105 series reserves the register settings, its internal state may change if excessive ambient noise is inserted. Measures are required to prevent noise generation or influence in terms of mounting and the system itself.
② It is recommended that you set the software to refresh the operating state (register reset) periodically to avoid spike noise.

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